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ROBUST SEQUENTIAL DESIGN OF DECENTRALIZED CONTROLLERS

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1 Introduction

Decentralized control remains popular in the chemical process industry, despite developments of advanced controller synthesis procedures leading to full multivariable controllers. Some reasons for the continued popularity are ease of implementation and maintainance, failure tolerance and operator acceptance. The design of a decentralized control system consists of two main steps:

a) Control structure selection, that is, choosing manipulated inputs and controlled outputs, and pairing inputs and outputs.

b) Design of a single-input single-output (SISO) controller for each loop.

In this paper we will consider Step b), and assume that Step a) has already been completed (e.g. by using tools such as the RGA [9, 10]). Standard controller synthesis algorithms (e.g. H_2 or H_∞ synthesis) lead to multivariable controllers, and cannot handle requirements for controllers with a specified structure. Instead, some practical approaches to the design of decentralized controllers have evolved:

- Independent design [12, 15, 11, 3].
- Simultaneous design using parameter optimization.
- Sequential design [5, 13, 14].

In this paper we discuss sequential design in detail and present some new results.

Notation. The matrix $G(s)$ denotes a square plant of dimension $n \times n$, and $g_{ij}(s)$ is the ij'th element of $G(s)$. The decentralized controller is assumed to be diagonal with diagonal elements $c_i(s)$ (see Fig. 1). The matrix consisting of the diagonal elements of G is denoted $\tilde{G} = \text{diag}\{g_{ii}\}$. The sensitivity function is

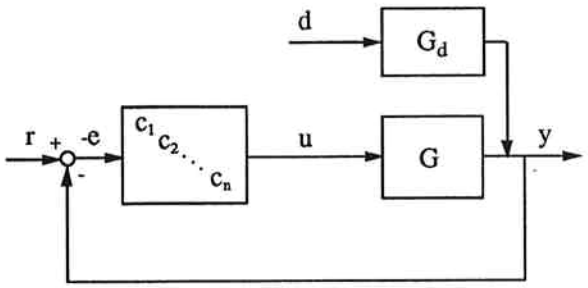

Figure 1: Block diagram of feedback system with decentralized controller.

$S = (I + GC)^{-1}$ and the complementary sensitivity is $H = I - S = GC(I + GC)^{-1}$. Loop i is the SISO feedback system consisting of g_{ii} and c_i. The sensitivity functions and complementary sensitivity functions for the individual loops are collected in the diagonal matrices $\tilde{S} = \text{diag}\{\tilde{s}_i\} = \text{diag}\{1/(1 + g_{ii}c_i)\} = (I - \tilde{G}C)^{-1}$ and $\tilde{H} = \text{diag}\{\tilde{h}_i\} = \text{diag}\{g_{ii}c_i/(1+g_{ii}c_i)\} = \tilde{G}C(I-\tilde{G}C)^{-1}$. Two frequency-dependent measures which we make use of are the Performance Relative Gain Array, PRGA $= \Gamma = \tilde{G}G^{-1}$ (with elements γ_{ij}), and the Closed-Loop Disturbance Gain, CLDG $= \tilde{G}G^{-1}G_d$ (with elements δ_{ik}).

2 Sequential Design

Sequential design involves closing and tuning one loop at the time. The procedure was introduced in the control literature by Mayne [13], but it is probably fair to say that it has always been the most common way of designing decentralized controllers n industry, and it has been addressed by several other authors (e.g. [2, 4, 5, 13, 14, 17]).

Advantages with sequential design

1. Each step in the design procedure involves designing only one single input single-output (SISO) controller.

2. A limited degree of failure tolerance is guaranteed: If stability has been achieved after the design of each loop, then the system will remain stable if loops fail or are taken out of service in the reverse order of how they were designed.

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Problems with Sequential Design

1. The final controller design, and thus the control quality achieved, may depend on the order in which the controller in the individual loops are designed.

2. Only one output is usually considered at the time, and the closing of subsequent loops may alter the response of previously designed loops, and thus make iteration necessary.

3. The transfer function between input u_k and output y_k (which is considered when designing loop k) may contain right half plane (RHP) zeros that do not correspond to RHP transmission zeros of $G(s)$.

The usefulness of a sequential design procedure will depend on how successfully it adresses the above issues. The conventional rule for dealing with problem 1 is to close the fast loops first, the reason being that the loop gain and phase in the bandwidth region of the fast loops is relatively insensitive to the tuning of the slower loops. While this argument is reasonable for *loop k* itself (involving only r_k, u_k and y_k), the response of *output k* may still be sensitive to the tuning of the controller in a slower loop l, if u_l has a large effect on y_k.

We will attempt to reduce the severity of problem 2 by using simple estimates of how the undesigned loops will affect the output of the loop to be designed.

Problem 3 may affect the order of loop closing since we will require that the system is stable after the closing of each loop.

3 A New Design Procedure

3.1 Initializing the Design Procedure

Consider the feedback system in Fig. 1. The control error (offset) is given by

$$e = y - r = -Sr + SG_d d \tag{1}$$

Assume that the plant transfer function G and the disturbance transfer function G_d are scaled such that the largest tolerable offset (e) in any controlled variable has magnitude 1 and the largest individual disturbance (d) expected has magnitude 1 at any frequency. For simplicity we assume that the largest expected changes in the setpoints (r) are equal to the allowed magnitude of e. To satisfy our performance objectives, we must then for any single setpoint $|r_j| < 1$ at least require

$$|[S]_{ij}| < 1 \tag{2}$$

and for any single disturbance $|d_k| < 1$ at least require

$$|[SG_d]_{ik}| < 1 \tag{3}$$

(here $[A]_{ij}$ denotes the ij'th element of A). We want to express these performance requirements in terms of the individual designs. We first factorize the sensitivity S in terms of the sensitivity of the individual designs, $\tilde{S} = (I + \tilde{G}C)^{-1}$:

$$S = (I + GC)^{-1} = \tilde{S}(I + E_H\tilde{H})^{-1} \tag{4}$$

where $E_H = (G - \tilde{G})\tilde{G}^{-1}$. For frequencies ($\omega < \omega_B$) below the bandwidths of the individual loops we have $\tilde{H} \approx I$ and we get $(I + E_H\tilde{H})^{-1} \approx \tilde{G}G^{-1} = \Gamma$. The control error becomes

$$e = y - r \approx -\tilde{S}\Gamma r + \tilde{S}\Gamma G_d; \qquad \omega < \omega_B \tag{5}$$

$\Gamma = \{\gamma_{ij}\}$ is known as the Performance Relative Gain Array (PRGA) and $\Gamma G_d = \{\delta_{ik}\}$ is the Closed Loop Disturbance Gain (CLDG) [9, 16]. At frequencies $\omega < \omega_B$ we also have $\tilde{S} \approx (\tilde{G}C)^{-1}$ and the performance requirements in Eqs. (2) and (3) become for $\omega < \omega_B$

$$\text{PRGA}: \quad \left|\frac{\gamma_{ij}}{g_{ii}c_i}\right| < 1 \quad \Leftrightarrow \quad |g_{ii}c_i| > |\gamma_{ij}| \tag{6}$$

$$\text{CLDG}: \quad \left|\frac{\delta_{ik}}{g_{ii}c_i}\right| < 1 \quad \Leftrightarrow \quad |g_{ii}c_i| > |\delta_{ik}| \tag{7}$$

Thus $|\gamma_{ij}(j\omega)|$ is the minimum loop gain requirement at frequency $\omega < \omega_B$ for a change in setpoint j to cause an acceptably small offset in output i. Likewise, $|\delta_{ik}(j\omega)|$ is the minimum loop gain requirement at frequency $\omega < \omega_B$ in loop i for rejecting disturbance k. In other words, from frequency dependent plots of $|\gamma_{ij}|$ and $|\delta_{ik}|$, we can get a good estimate of the required bandwidth in the individual loops. We will therefore use the PRGA and CLDG for two purposes:

1. Determine the *order* of loop closing (closing first loops that are required to be fast).

2. Estimate loop gain requirements $|g_{ii}c_i|$ for counteracting interactions and disturbances, thereby finding an estimate of the complementary sensitivity functions ($\tilde{h}_i$'s) for the individual loops.

3.2 Refined Loop Gain Requirements

The above relationships may be used to independently design each loop in terms of performance, at least at lower frequencies. However, when the controllers in some loops have been designed, we have gained more knowledge about the closed loop system, and we want to take advantage of this new knowledge when designing subsequent loops.

In the following, we will assume without loss of generality that the loops are closed (and controllers designed) in the order $1, 2, \cdots, k, k+1, \cdots$, and that the loop to be designed is k. Let G_k denote the submatrix of dimension $k \times k$ in the upper left corner of G, let $C_k = diag\{c_1, c_2, \ldots, c_k\}$ and let $S_k = (I + G_kC_k)^{-1}$ and $H_k = G_kC_k(I + G_kC_k)^{-1}$. Introduce $\hat{G}_k = \text{diag}\{G_k, g_{ii}\}$,

$\hat{S}_k = \text{diag}\{S_k, \tilde{s}_i\}$, and $\hat{H}_k = \text{diag}\{H_k, \tilde{h}_i\}$, $i = k+1, k+2, \cdots, n$.

We then have the following generalization of Eq. (4)

$$S = \hat{S}_k(I + E_k\hat{H}_k)^{-1}; \quad E_k = (G - \hat{G}_k)\hat{G}_k^{-1} \qquad (8)$$

which is the basis for our design procedure. Note that:

1. For $k = 1$ we have $\hat{G}_1 = \tilde{G}$, $\hat{S}_1 = \tilde{S}$ and $\hat{H}_1 = \tilde{H}$ and rederive (4).

2. $S_k = (I + G_kC_k)^{-1}$, the upper left $k \times k$ block of $\hat{S}_k$, yields the response for loops 1 to k with the remaining loops *open*.

3. On the other hand, the upper left $k \times k$ block of S yields the response of loops 1 to k with the remaining loops *closed*. Thus, we get from Eq. (8) that rows 1 to k of $(I + E_k\hat{H}_k)^{-1}$ express how interactions from loops $i > k$ affect loops 1 to k.

4. $(I+E_k\hat{H}_k)^{-1}$ is in general a full matrix. To evaluate this matrix we will use an estimate of $\tilde{h}_i$ for the loops that have yet not been designed.

5. In our sequential design procedure we will consider the first k rows of $(I + E_k\hat{H}_k)^{-1}$ as an *input weight* for performance to $S_k = (I + G_kC_k)^{-1}$.

3.3 The Sequential Design Procedure

The proposed sequential design procedure is outlined here. The objective of the controller design is to design SISO controllers c_i that minimize some performance objective. As the performance objective we usually consider a norm (e.g, H_∞-norm or H_2-norm) of the weighted sensitivity function of the overall system, and get the following design problem:

$$\min_{c_i} \| W_PSW_D \| \qquad (9)$$

The performance weights $W_P^{n_P \times n}$ and $W_D^{n \times n_D}$ need not be square, but W_P is often a square diagonal matrix used to weigh each individual output.

Note that S can be expressed in terms of $\hat{S}_k$ as shown in Eq. (8). Obviously, we can only have a performance requirement for an output where we have a controller. For this reason, define

$$W_{Pk}^{n_P \times k} : \text{ first } k \text{ columns of } W_P \qquad (10)$$

Likewise, define

$$W_{Dk}^{k \times n_D} : \text{ first } k \text{ rows of } (I + E_k\hat{H}_k)^{-1}W_D \qquad (11)$$

- *Our sequential design procedure is then for step k to design a SISO controller c_k that minimizes $\|W_{Pk}S_kW_{DK}\|$ where S_k depends on c_k, and W_{Dk} is evaluated using an estimate of $\tilde{h}_i$ for $i \geq k$.*

The main steps are as follows:

Step 0. Initialization: Determine the order of loop closing and estimate $\tilde{H} = \text{diag}\{\tilde{h}_i\}$. The loop gain requirements given in Section 3.1 in terms of the PRGA and CLDG are helpful for this purpose, as will be demonstrated in the example.

Step 1. Design of controller c_1 by considering output 1 only. We have $\hat{G}_k = \tilde{G} = \text{diag}\{g_{ii}\}$ and $\hat{H}_k = \tilde{H}$. W_{P1} is the first column of W_P, and W_{D1} is the first row of $(I + E_k\tilde{H})^{-1}W_D$.

Step k. Design of controller c_k by considering outputs 1 to k. Here $\hat{G}_k = \text{diag}\{G_k, g_{ii}\}$; $i = k+1, \cdots, n$. We use $\hat{H}_k = \text{diag}\{H_{k-1}, \tilde{h}_i\}$; $i = k, \cdots, n$, where H_{k-1} is the complementary sensitivity function for the $k-1$ loops that have been designed and $\tilde{h}_i$ is the estimate from Step 0 for the loops that are yet to be designed.

Step n. Design of the last controller c_n. This is done by considering the overall problem in (9).

Remarks:

1. The design procedure may be generalized to cases where we consider closed-loop transfer functions other than S.

2. With the possible exception of Step 0, the procedure is easily automated.

3. $S_k = (I + G_kC_k)^{-1}$ is required to be stable at each step in the design. This guarantees the limited degree of failure tolerance mentioned in Section 2.

4. With the exception of Step n, we use the estimate of $\tilde{h}_k$ to evaluate $\hat{H}_k$ (and W_{Dk}) during the design of c_k. This is not strictly necessary, but making $\tilde{h}_k$ a function of c_k will complicate the setup of the controller design problem.

5. One objective with our procedure is that the use of the input weight W_{Dk} (using the estimate of $\tilde{h}_i$ for $i \geq k$) should reduce the need for iteration (redesigning loops), and this has indeed been confirmed by examples.

6. In the example we use an H_∞ performance objective,

$$\| W_PSW_D \| = \| W_PSW_D \|_\infty = \sup_\omega \bar{\sigma}(W_PSW_D) \qquad (12)$$

7. In the example we also include model uncertainty. Then for robust performance (12) should be satisfied for all possible S's allowed for by the uncertainty description. With H_∞-bounded model uncertainty this may be reformulated as an equivalent structured singular value test. For example, for the case with multiplicative input uncertainty (see Fig. 2) we get the robust performance condition (e.g. [15])

$$\mu_\Delta \begin{bmatrix} W_ICSG & W_ICSW_D \\ W_PSG & W_PSW_D \end{bmatrix} < 1, \quad \forall\omega \qquad (13)$$

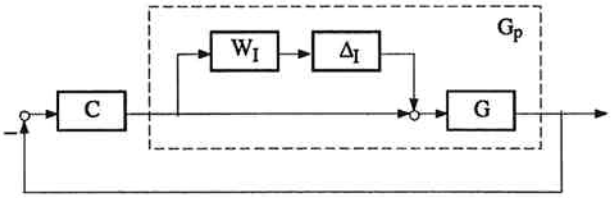

Figure 2: Multiplicative input uncertainty.

where μ is the structured singular value [6] and $\Delta = \text{diag}\{\Delta_I, \Delta_P\}$. Δ_I is a diagonal matrix representing the input uncertainty, and Δ_P is a full matrix representing the performance requirement. Our sequential design procedure is then for step k to design a SISO controller that minimizes

$$\mu_{\Delta_k}\begin{bmatrix} W_{Ik}C_kS_kG_k & W_{Ik}C_kS_kW_{Dk} \\ W_{Pk}S_kG_k & W_{Pk}S_kW_{Dk} \end{bmatrix} \qquad (14)$$

with $\Delta_k = \text{diag}\{\Delta_{Ik}, \Delta_P\}$. Here Δ_{Ik} a diagonal $k \times k$ matrix and Δ_P is a full $n_D \times n_P$ matrix.

8. Although our design procedure is new, the idea of using a simplified estimate of the effect of closing the other loops is not new. For example, Balchen and Mummé ([1], Appendix C) derive an estimate the transfer function in loop k using an estimate of $\tilde{h}_i$ for the other loops, and use this to find pairings.

9. It is easier to estimate the complementary sensitivity function for the individual loops than to estimate the controller in the individual loops. This holds especially at low frequency, where control is almost perfect, and we know that $\tilde{h}_i \approx 1$.

10. For the examples we have studied, the sequential design procedure presented in this paper achieved a control quality almost equivalent to that achieved using parameter optimization for all loops simultaneously.

11. A choice has to be made as to what design method should be used for design of the SISO controllers. Alternatives are synthesis (with no restriction on the controller parameterization) and parametric optimization (with a fixed controller parametrization). The disadvantage with synthesis, for example using the H_2- and H_∞-norms, is that the controller order becomes very large. We therefore prefer parameter optimization which yields simple low-order controllers, e.g., a PID controller. Parameter optimization is managable when we employ sequential design because we consider only one controller at the time. The main disadvantage is that the achievable control quality depends on the controller parameterization.

4 Example

Consider the following example from Chiu [4]. The plant is given by

$$G(s) = \begin{bmatrix} \frac{0.66}{6.7s+1} & \frac{-0.61}{8.4s+1} & \frac{-0.005}{9.06s+1} \\ \frac{1.11}{3.25s+1} & \frac{-2.36}{5s+1} & \frac{-0.01}{7.09s+1} \\ \frac{-34.7}{8.15s+1} & \frac{46.2}{10.9s+1} & \frac{0.87(11.61s+1)}{(3.89s+1)(18.8s+1)} \end{bmatrix} \qquad (15)$$

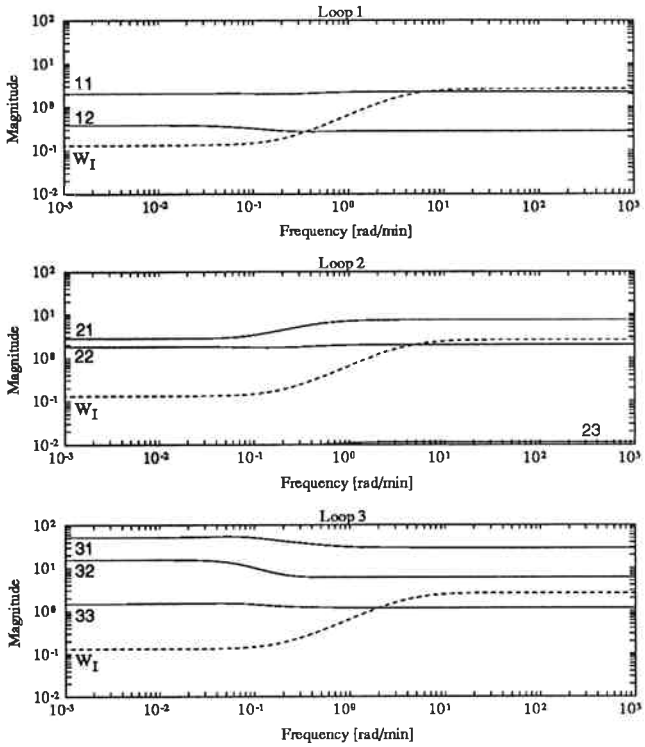

Figure 3: Elements of PRGA $= \tilde{G}G^{-1}$ (solid lines) and uncertainty weight (dotted line). PRGA_{13} is smaller than 10^{-2} at all frequencies.

The outputs are assumed to be scaled correctly with respect to each other. We immediately note the strong one-way interaction in the system represented by the large off-diagonal elements in row three. In [4] only robust stability is considered, with independent, multiplicative input uncertainty (see Fig. 2) with uncertainty weight $W_I(s) = 0.13\frac{5s+1}{0.25s+1}I$. This uncertainty weight reflects a steady state gain uncertainty of 13% and a maximum neglected time delay of 0.5 minute. We add the performance requirement $\bar{\sigma}(W_PS) < 1 \quad \forall\omega$, which should be satisfied for all possible plants allowed by the input uncertainty. We choose the performance weights

$$W_D = I; \quad W_P = w_PI; \quad w_P(s) = 0.4\frac{\tau_{cl}s+1}{\tau_{cl}} \qquad (16)$$

The objective is to make the system as fast as possible in a robust sense, by minimizing τ_{cl} in the performance weight subject to $\mu_{RP}(M) < 1$ (μ_{RP} meaning μ for robust performance), where M is as given in Eq. (13).

We choose to pair on the diagonal elements of G as in [4]. We first want to estimate the required bandwidth, ω_i, in each loop.

The PRGA for this example is shown in Fig. 3 (solid lines), together with the uncertainty weight (dashed lines). PRGA elements larger than 1 imply interactions, and the figure shows that there is as expected severe interaction from loops 1 and 2 into loop 3. The loop gain in loop 3 must consequently be high at the frequencies where the feedback in loops 1 and 2 is effective to reject

the "disturbances" entering from loops 1 and 2. This means that the bandwidth in loop 3 has to be higher than the bandwidths in loops 1 and 2.

The bandwidth in loop 3 will be limited by the time delay of 0.5 minutes allowed by the input uncertainty. We therefore estimate $\omega_3 = 1$ [rad/min], which is slightly below the frequency where $|W_I|$ crosses one.

Next consider the "disturbance" from loop 1 into loop 3, as expressed by the PRGA element γ_{31}. We have $\gamma_{31} \approx 50$ for frequencies lower than approximately 0.1 [rad/min]. Thus, at the bandwidth frequency for loop 1, ω_1, we must require $|g_{33}c_3(j\omega_1)| > 50$. If $|g_{33}c_3|$ has a slope of -2 on the Bode magnitude plot, we get $\omega_1 < 1/\sqrt{|\gamma_{31}|} = 1/7.1$. A similar discussion applies for the interaction from loop 2 into loop 3. We have $|\gamma_{32}| \approx 10$ at low frequencies, and if $|g_{33}c_3|$ has a slope of -2 we get $\omega_3 < 1/\sqrt{|\gamma_{32}|} \approx 1/\sqrt{10}$. For the interactions of loop 1 and loop 2 into loop 3 to be of equal significance, we thus get that $\omega_2/\omega_1 = \sqrt{|\gamma_{31}|/|\gamma_{32}|} \approx \sqrt{5}$, and this will be used in the following.

From the above discussion the controller parametrization is chosen to allow a high roll-off

$$c_i(s) = k\frac{T_1 s + 1}{T_1 s}\frac{T_2 s + 1}{10T_2 s + 1} \tag{17}$$

Note that this is not strictly a PID controller since the pole in the last term is at a lower frequency ($s = 0.1/T_2$) than the zero.

Step 0: From the above discussion we conclude that the order of loop closing should be: Loop 3 (fastest), loop 2, loop 1. The initial estimates for the complementary sensitivity functions for the individual loops are chosen to be second order of the form

$$\tilde{h}_i(s) = \frac{1}{(\frac{s}{\omega_i} + 1)^2} \tag{18}$$

As estimates of the loop bandwidths ω_1, ω_2 and ω_3, we select based on the above discussion the following:

1. Loop 3 is the fastest and we estimate $\omega_3 = 1$ [rad/min].
2. $\omega_2/\omega_1 = \sqrt{5} \approx 2.2$.
3. $\omega_1 = 1/\tau_{cl}$ where τ_{cl} is minimized at each step such that $\mu = 1$. This choice follows since loop 1 is the slowest loop, and has little interactions from the other loops. Thus the response of this loop by itself will determine the performance of the overall system.

Step 1: Controller design for loop 3. W_{D1} is the third row of $(I + E_k\hat{H}_k)^{-1}$, and there is one 1×1 perturbation block for the input uncertainty, and one 3×1 perturbation block for the performance specification. Iterating on τ_{cl} (and changing ω_1 and ω_2 correspondingly, as explained above) we obtain $\mu = 1.0$ for $\tau_{cl} = 8.5$ [min], and the corresponding controller is

$$c_3(s) = 84.9\frac{4.70s + 1}{4.70s}\frac{4.01s + 1}{40.1s + 1} \tag{19}$$

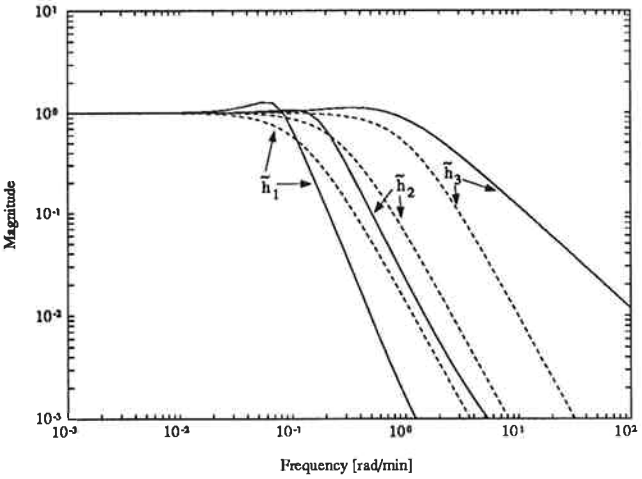

Figure 4: Complementary sensitivity functions for the individual loops, $\tilde{h}_i$. Solid: Final designs. Dotted: Estimates at Step 1 of the design ($\omega_1 = 1/8.5$, $\omega_2 = 2.2\omega_1$, $\omega_3 = 1$).

Step 2: Loop 2. In $\hat{H}_k$ we replace the estimate of $\tilde{h}_3$ by the actual design for loop 3. W_{D2} is the second and third rows of $(I + E_k\hat{H}_k)^{-1}$. There is one diagonal perturbation block of dimension 2×2 for the input uncertainty, and a 3×2 perturbation block for performance. $\mu = 1.0$ is obtained for $\tau_{cl} = 11$ [min], with

$$c_2(s) = -0.079\frac{1.32s + 1}{1.32s}\frac{0.186s + 1}{1.86s + 1} \tag{20}$$

Step 3: Loop 1. Now all loops are included and we consider the overall design problem with a diagonal 3×3 perturbation block for the input uncertainty and a full 3×3 perturbation block for performance. $\mu = 1.0$ is obtained for $\tau_{cl} = 18$ [min] with

$$c_1(s) = 0.04\frac{0.385s + 1}{0.385s}\frac{0.898s + 1}{8.98s + 1} \tag{21}$$

Note that τ_{cl} which was obtained in the last step, is the value of τ_{cl} which will apply to all outputs in the overall problem. In comparison, the best decentralized controller found using simultaneous parametric optimization with the same controller parametrization gave $\mu = 1$ for $\tau_{cl} = 16$ [min]. This demonstrates that there is little to be gained by iterating on the design.

The final complementary sensitivity functions (solid lines) for the individual loops, $\tilde{h}_i$ are shown in Fig. 4, together with the estimates (dotted lines) used in Step 1 of the design. These differer considerably, and this illustrates that the design method does not require very accurate à priori estimates of $\tilde{h}_i$.

In Fig. 5a we show the response to a unit setpoint change in output 1 (the most difficult direction). The interactions are pronounced, but acceptable. As seen from the dashed lines the responses are insensitive to adding 0.5 min time delay in all channels.

Comparison with conventional design. For this example, conventional sequential design, e.g. based on Ziegler

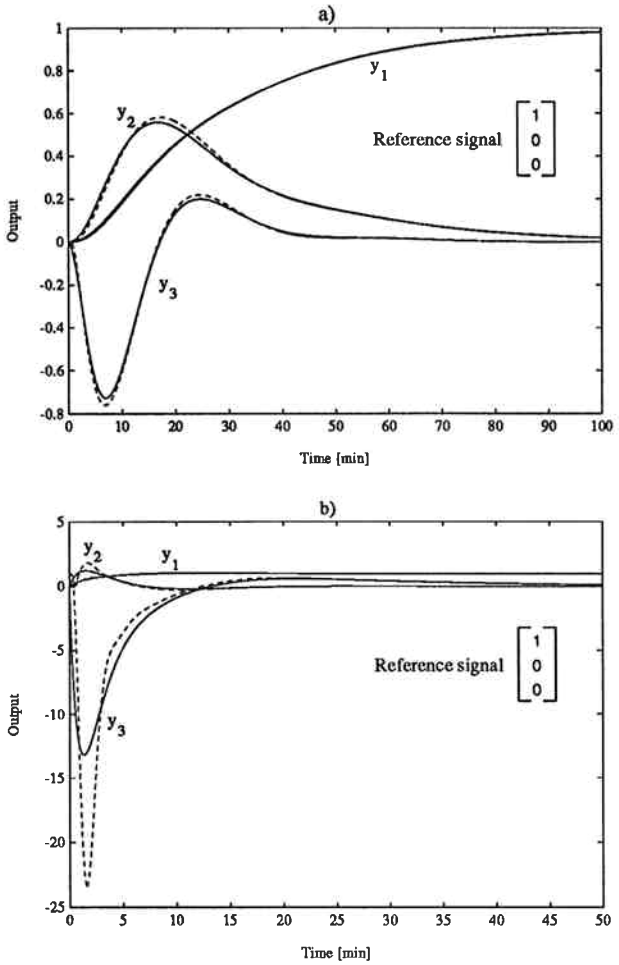

Figure 5: Responses with decentralized control. a) Sequential design. b) BLT-detuned Ziegler-Nichols PI tunings (note scale on y-axis). Solid: Nominal responses. Dotted: 0.5 min. time delay on inputs.

Nichols tunings, will yield unacceptable designs, because conventional sequential design only considers one output at the time. Thus, there is no incentive for restricting the bandwidths of loops 1 and 2 in order to avoid interactions into loop 3. This is seen from the simulations in Fig. 5b where we use the BLT PI-tunings of Luyben [12], which are based on detuning the Ziegler Nichols tunings by a common factor for all loops.

5 Conclusion

We propose a new sequential design procedure, that involves minimizing the design criterion at each individual step. The key basis for our design procedure is the factorization of the overall system in terms of the individual designs, Eq. 8, and the use of estimates for the complementary sensitivity functions, $\tilde{h}_i$, of the loops that are yet to be designed. By use of measures such as the PRGA and CLDG we are able to obtain good initial estimates of the required loop gains, $g_{ii}c_i$, in the bandwidth region, and thus estimate $\tilde{h}_i = g_{ii}c_i/(1+g_{ii}c_i)$.

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