

Control for High Heat Chips' Cooling Based on Power Consumption and Temperature Signals

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Abstract—For CPU chips' cooling task, existing mono-variable control system has the defects of delay, fluctuation and high energy consumption. With the trend of multi-core and high frequency work pulse in CPU chips, traditional system does not fit for future cooling task. Several approaches such as chips' dissipated power nonlinear feed-forward, core temperature tracking and surface temperature feed-back are applied to improve control system. Simulations prove that comparing with the traditional out-core temperature based mono-input-output proportion tracking strategy, the improved system can bring better quality and energy-saving results. Also, the new system has parameters adaptability.

Keywords—CPU chip; temperature; cooling; control; power dissipation; usage rate; feed-forward

I. INTRODUCTION

In future space mission, more and more high heat integrated circuit chips need to be cooled [1]. Promoting the quality of high heat IC chips' cooling control is just a new study focus. CPU chips are a typical kind of high heat chips and their cooling control is the key of guaranteeing their stability and dynamic properties [2]. Traditional cooling control systems are mono-variable tracking system, and they apply proportional algorithm as control strategy [3-5]. That is, the discrete values of out-core temperature in chip are multiplied by a coefficient and then are used to adjust cooling actuator's driving power.

CPU chip is a body with inside heat sources. Its heat generating mechanism [6-9] makes temperature in chip is a nonstationary random process with delay and many influence factors. This is the bottle-neck for traditional control system to fit for future CPU chips' cooling task. Concretely speaking, uncertain deviation between out-core temperature measuring

values and real temperature [7], single system input variable and simple tracking control strategy, and so on, are main reasons. So, it is urgent to find new control system to cope with future challenges. Unluckily, trends of more cores and higher frequency of main pulse of CPU chip, future scheduling strategy of operating system, development of CPU internal structures and techniques, even increasing of cooling actuator's efficiency, will make CPU chip's power, heat and temperature more complex than expected.

To promote the transient and steady state quality of chip's surface temperature, this paper suggests a new system which combines several approaches such as new signals and their processing, more control algorithms and more complicated strategies. In the new system, CPU usage rate which indicates the chip's dissipated power in advance [9-11], and CPU core temperature which is more accurate and more sensitive and no delay, are used as inputs. And, power feed-forward, core temperature tracking and surface temperature feed-back strategies are added. Numerical simulation proved our new method is effective and advanced.

II. CHIPS' COOLING AND TRADITIONAL CONTROL SYSTEMS

Traditional cooling control system (seeing Fig. 1) uses analogue variables as inputs. It applies proportional strategy in Fig. 2 to determine the excitation voltage V_{out} of the cooling actuator, usually one or two air fan, as follows:

$$V_{out} = k_p T(t) \quad (1)$$

It is obvious that the object itself is not complex. That is, the chip's heat transfer delay and the air fan's cooling time are

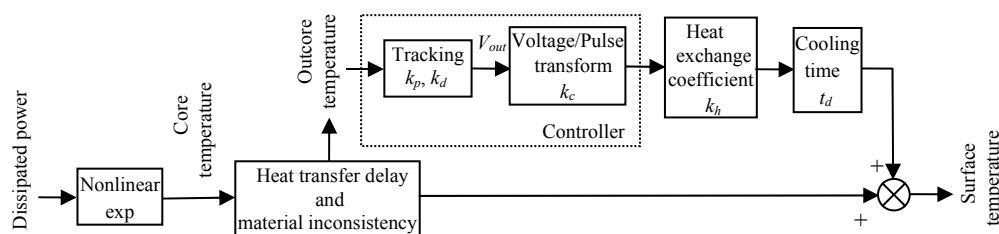


Figure 1. CPU chips' cooling model of tracking control system.

common properties in control systems. But there is peculiar complexity resulting from the nonstationary random and anisotropic inconsistency in temperature field. As being seen in Fig. 3, not only is there nonstationary random in out-core temperature and core temperature, but at least 1 second of time delay and at least 1°C of temperature variance in them as well. Besides, the uncertainty of heat resulted from CPU workloads and the variant cooling time influenced by heat exchanging efficiency of actuator, etc., bring the chips' cooling with difficulties.

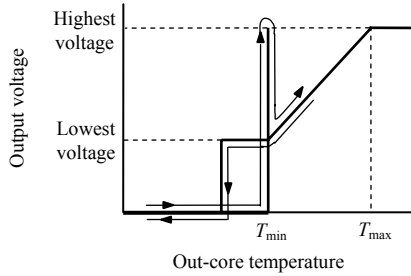


Figure 2. Traditional proportional tracking strategy.

Generally speaking, the traditional proportional tracking strategy cannot further improve the cooling control quality, and cannot face future challenges.

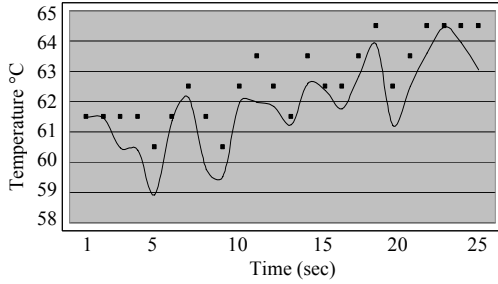


Figure 3. CPU core temp. & out-core temp.

III. MODEL OF CONTROL SYSTEM WITH DISSIPATED POWER FEED-FORWARD AND MULTI-TEMPERATURE PID

A. Improved Model of Controller

We noticed that chip's power consumption is in advance to its temperature. On the basis of existing tracking system, we introduce usage feed-forward to reflect the action of CPU's power consumption to temperature. Besides, we substitute out-core temperature with core temperature as input variable, and add algorithms of tracking and feed-back. Certainly, we take short window mean value from sequences of core temperature

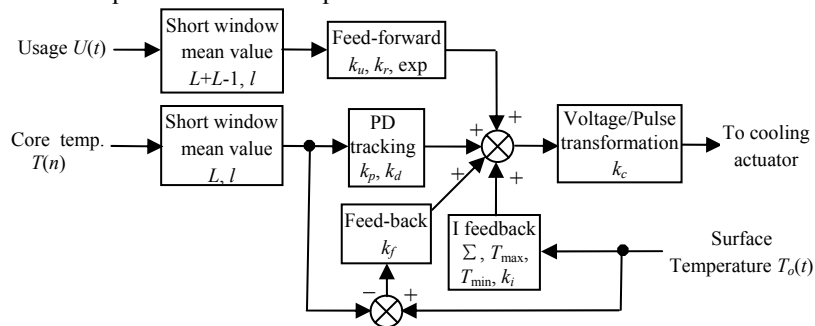


Figure 4. Improved model of CPU chip cooling controller.

and usage. Fig. 4 is the improved control system model. In Eq. (2) are several algorithms in the new model such as usage sequence nonlinear feed-forward, core temperature tracking, surface temperature feed-back, etc. In that equation, k_u is usage feed-forward coefficient and the linear item, k_r , is added to make up the attenuation with usage increasing. The k_p , k_i and k_d are proportional, integral and deviational coefficients of PID algorithm, respectively. The k_f is coefficient of different value feed-back.

$$\begin{aligned}
 & k_u \left\{ 1 - \exp\left(-E[U_n^{L,l}]\right) + k_r E[U_n^{L,l}] \right\} \\
 & k_p E[T_n^{L,l}] + k_d \frac{\left\{ E[T_n^{L,l}] - E[T_{n-1}^{L,l}] \right\}}{l} \\
 & k_i \sum_{i=1}^n \left\{ T_o(n) - \frac{T_{\max} + T_{\min}}{2} \right\} \\
 & k_f \left\{ T_o(n-1) - E[T_n^{L,l}] \right\}
 \end{aligned} \quad (2)$$

In Eq. (2), $E[U_n^{L,l}]$ and $E[T_n^{L,l}]$ are short window mean value of usage sequence and core temperature sequence, respectively.

B. Nonlinear Relation between Usage Rate and Core Temperature

The CPU usage measures microprocessor's workloads. It reflects the power consumption of chip directly and determines the amount of heat generated in the chip [7, 10-11]. For a CPU chip, suppose it gains heat Q_{gained} from its environment, $Q_{transfer}$ is the amount of heat transferred to it during a period of time and $Q_{component}$ is the amount of heat produced by running programs during a period of time. This can be expressed as [10]:

$$\begin{aligned}
 Q_{gained} &= Q_{transfer} + Q_{component} = \\
 & k(T_{out} - T_{source})t + [P_{base} + (P_{\max} - P_{base})u]t
 \end{aligned} \quad (3)$$

where T_{source} is core temperature and T_{out} is air temperature, P_{base} is the power consumption when CPU is idle and P_{\max} is the consumption when chip is fully utilized, u is usage rate.

Since $\Delta T = \frac{1}{mc} \Delta Q$, then

$$\begin{aligned} \frac{dQ_{gained}}{dt} + k(T_{source} - T_{out}) &= P_{base} + (P_{max} - P_{base})u \\ mc \frac{d(T_{source} - T_{out})}{dt} + k(T_{source} - T_{out}) &= P_{base} + (P_{max} - P_{base})u \end{aligned} \quad (4)$$

where m is the mass of chip, c is its heat capacity, and k is related to m and c .

In Fig. 5 is statistic result of real out-core temperature measuring values. When usage is larger than 10%, the action of dissipated power to out-core temperature can be seen easily. Through fitting, we get the relation between steady temperature values and constant usage values as Eq. (5), where T_{base} is the basic temperature corresponding to zero usage, k_u and k_r are constants. It must be pointed out that Eq. (5) just coincides with the solution form of Eq. (4).

$$T(\infty) = T_{base} + k_u(1 - e^{-k_r u}) \quad (5)$$

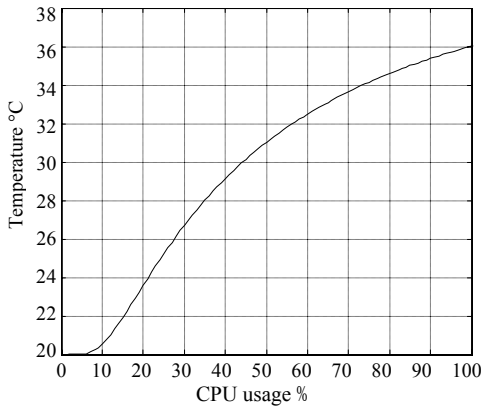


Figure 5. Steady temperature under different usage.

C. Short Window Mean Value of Core Temperature and Usage Sequences

The discrete sequence of core temperature $\{T_n\}$ is a nonstationary random one with big sampling cycle. It can be proved that the short window mean value of the sequence $\{E[T_n^{L,l}]\}$ contains the same heat as $\{T_n\}$. And, the waveform of the former is smoother than that of the latter. This means short window mean value is more fittable for being applied to cooling control than discrete values.

Brief proof:

Let frame length L is 2, frame width l is 1, then $\{E[T_n^{L,l}]\}$ contains heat

$$Q_{aver} = \sum_{i=1}^n \int_{i-1}^i T_i dt = \frac{T_1}{2} + \sum_{i=1}^n \int_i^{i+1} \frac{T_i + T_{i+1}}{2} dt + \frac{T_n}{2}. \text{ And } \{T_n\}$$

contains heat $Q_{disc} = \frac{T_1}{2} + \sum_{i=1}^n \int_i^{i+1} \frac{T_i + T_{i+1}}{2} dt$, if n is large

enough, $Q_{aver} \approx Q_{disc}$. Furthermore, if $T_{i+1} > T_i$, then $T_{i+1} > \frac{T_i + T_{i+1}}{2}$, if $T_{i+1} < T_i$, then $T_{i+1} < \frac{T_i + T_{i+1}}{2}$. **Proof end**

As for usage sequence, $U(n)$, we make use of its short window mean value $\{E[U_n^{L,l}]\}$, too.

IV. SIMULATION AND ANALYSIS

A. Selection of Parameters

For simplicity, we suppose the power dissipated by cooling driving actuator is all used for cooling. According to experiment experiences, let cooling time, t_d , is 1 second, and time constant of heat transfer, τ , is 0.25 second. That means all heat generated from source is taken away to environment by cooling actuator in 1 second.

All parameters' values are taken as follows: $L=2$, $l=1$, $\tau=0.25s$, $t_d=1s$, $(T_{min}, T_{max})=(50^\circ C, 70^\circ C)$, $(U_{min}, U_{max})=(8V, 12V)$, $k_p=0.1$, $k_i=0.01$, $k_d=0.01$, $k_f=0.01$, $k_c=1.2$, $k_h=8$, $k_u=0.1$, $k_r=1.0$.

B. Simulation Results and Analysis

1) *Comparisons between core temperature and out-core temperature as input variable.* The simulation results of pure proportional tracking control (seeing Fig. 1) using out-core temperature or core temperature as inputs are showed in Fig. 6, respectively. Obviously, owing to the uncertainty and delay of out-core temperature, its result is much worse than that of core temperature. Simulation results indicate that the larger or smaller is k_p , the larger is the surface temperature's fluctuation amplitude. This is because the pure proportional tracking strategy can not eliminate the disturbance of uncertain deviation in out-core temperature values. In real application, the effect of k_p is the same as that of heat exchange coefficient of cooling actuator, this means that traditional strategy does not fit for cooling actuator with lower heat exchange efficiency, and not for actuator with higher heat exchange efficiency, either. It is needed to point out that out-core temperature used in our numerical calculating has smaller random deviation. Actual random deviation is bigger and its influence is more serious.

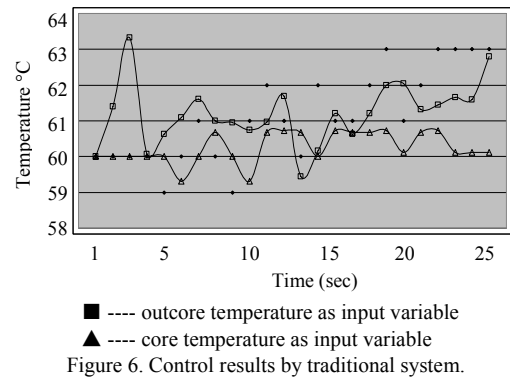
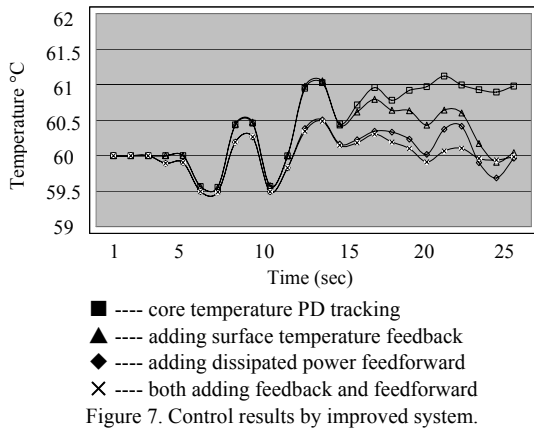


Figure 6. Control results by traditional system.

2) *Comparisons of control qualities made by different improved strategies.* For improved control system in Fig. 4, we use core temperature in Fig. 2 as input variable to do simulations. At the beginning, the controller only with PD core temperature tracking algorithm make surface temperature having 1°C steady state deviation. Then, after surface temperature feed-back being added, controller eliminates the deviation. Or, after usage nonlinear feed-forward being added, the overshoot of surface temperature is lower. Lastly, once surface temperature feed-back and usage feed-forward are added simultaneously, the result is best both in transient and steady state.(seeing Fig. 7)



3) *Comparison of power dissipated by cooling actuator.* For the combination strategy of core temperature tracking and surface temperature feed-back, the numerical calculating results of using two different values spent different energy. Control system using discrete values of core temperature makes the actuator spend 2.46053 Joule of energy, whereas system using short window mean values of core temperature makes the actuator spend 1.76581 Joule of energy. In our example, the former spends 0.69472 Joule more energy than the latter during 20 seconds.

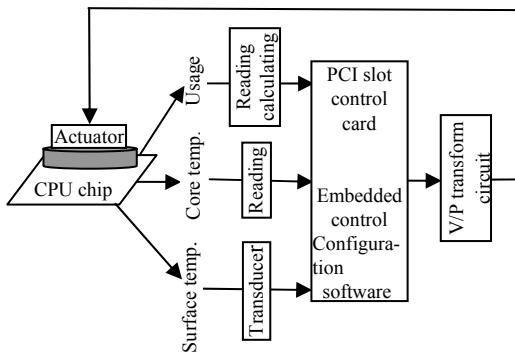


Fig. 8. A feasible realizing scheme of improved chip's cooling control system.

4) *Discussions about feasibility and practicability.* Simulating work indicates that the parameters in new system model such as k_p , k_i , k_d , k_f , k_u , k_r , L and l can be adjusted in wide range to cope with different values of τ , t_d , k_c , k_h . For instance, whether the cooling actuator is air fan or liquid pump or semiconductor thermoelectric patch, i.e., whether the

actuators' heat exchange efficiency is high or low, simulating shows our model can give excellent control quality. For example, under the circumstance of CPU core temperature behaving different random properties owing to different operating systems, or different main pulses, or different user softwares, new system can adapt them by using corresponding L and l .

V. CONCLUSION

This paper studied how to improve CPU chips' cooling control system and suggested several new methods in two aspects: one is of input signals and their processing; the other is of control strategies. Numerical calculating and simulating verified that usage sequence which indicates CPU power and core temperature sequence which is more accurate and more instant can avoid the disadvantages of out-core temperature values. Also, it was verified that power feed-forward and surface temperature feed-back can enhance system's functions and improve its performance. The improved control system has advantages in control quality, energy saving and adaptability. Our improved system can be easily realized by making use of existing techniques. Actually, it does be our coming work. Fig. 8 shows one feasible scheme of our improved control system.

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