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Testing device design for validation of synchronization between high speed camera and drop weight test machine

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***Abstract*—High-speed cameras are expanding into science laboratories in many disciplines. For example, they can be used for monitoring of the impact testing course, widely spread in evaluation of materials. Usually, they exhibit a slight delay between the trigger pulse was applied and the recording was started. For many applications, this delay may be critical. The authors of this paper have faced two problems: the need to determine the delay in total and the need to check whether it varies in time or not. Therefore, the hereby described device was designed. It allows measurement of the delay of the camera's start in the range from 1 to 999 ms with the step of 0.1 ms.**

Keywords—Synchronization, testing, high speed camera, drop weight test

I. INTRODUCTION

Impact testing has become commonly used as a method of evaluation of materials and structures. Force and acceleration are the most commonly measured parameters. The technologies for obtaining these parameters are mature enough. It is also important to define the sample deflection, which is not easily practicable at high deformation rates.

The authors of [1] and [2] used high speed camera for high strain-rate testing in their research. They fully discussed methods to synchronize high speed camera to conventional measurements at high speed effects, especially high strain-rate. Also a discussion about advantages and disadvantages of used measuring techniques has been provided.

According to [3], in the last decade, high speed digital visualization has made significant progress to many areas of impact testing. New generation of high speed cameras with metal oxide semiconductor (CMOS) sensors technology which allows frame rates in excess of 100 000 per second, albeit with decreased resolution. Sensors are more sensitive and they do not need too much light as last generation, in spite of image quality has improved noticeable.

As the high speed cameras have improved in time, they became a part of production line where are integrated in the machine with the visual function. Today processes are fast and high speed cameras guarantee fluent and quality production. Machine vision inspection technology uses contactless recording through sensors to quality product. It is possible to detect surface quality defects in automatic mode (online) [4].

In this paper, issues of application of high speed cameras in drop weight tests, as it is described on the next page, are considered. As it is described in the following text, time synchronization of the camera becomes critical at this kind of tests. However, the application range of high speed cameras is much wider.

For example, according to [5] it is possible to use the high speed camera as a device recording a high speed digital video for better vision of sample behavior. High speed video can offer to make sense of data measured on other channels and also high speed video can be useful for determination of cracks initiation and propagation and where delamination occurs. For verifying what it is measured on other channels, high-speed video can be also used, e.g. for checking that the data which were measured are the response of tested specimen and not for example of any supporting structures.

Common test for hand-held electronic product prototypes is a free-fall test, in which the difficulties on the impact orientation control are. H.L. Wang, S.C. Chen, L.T. Huang and Y.J. Wang dealt with drop tester with orientation repeatability for electronic products. They investigated the physics of a patented drop test platform with impact angle repeatability and developed a spatial orientation analytic algorithm. Using of charge coupled device (CCD), in comparison with high-speed camera (HSC), is that it has relatively good resolution for impact angle analysis and it is low cost and because of a patented methodology it is able to obtain two projected angles at the same time using only a single CCD and a mirror. From the mirror it is possible to derive a spatial orientation at impact instance. The repeatability of this tester is caused by four various drop orientation tests [6].

American scientists E.M. Hunt, S. Malcolm and M. Jackson investigated high-speed study of drop weight impact ignition of one material using infrared thermography. The device modified type 12 impact tester in conjunction with a FLIR SC6000 thermal imaging camera was used. Using this device, they could find out the material behavior under high thermal heating [7].

II. MOTIVATION

Drop weight test machine is used for evaluation of cracks and penetration into materials. Common practice is evaluation after testing process with the aid of macro- and microscopy. However, the process of crack propagation is important for evaluation of mechanical properties. Without synchronization between high speed camera and drop weight test machine, the process record gives us just information about visual observation. Although, precise synchronization between both apparatuses which ensures evaluation of machine parameters (such as impact force, bend of sample) in exact time of synchronized high speed record, there is required step to validate of synchronization process.

In order to establish synchronization between the high speed camera and the drop weight test machine (Fig. 1), a specialized synchronizing device has been constructed. The final arrangement of the measuring station is depicted in Fig. 2. However, when performing tests, an unpredictable delay between the synchronizing pulse and start of the high speed camera occurred. The high speed camera's datasheet did not specify any information on this kind of delay and also the manufacturer's service network was not able to provide us with relevant information on the camera's delay. The authors do intentionally not mention the manufacturer and type of the camera.

However, the following questions have arisen:

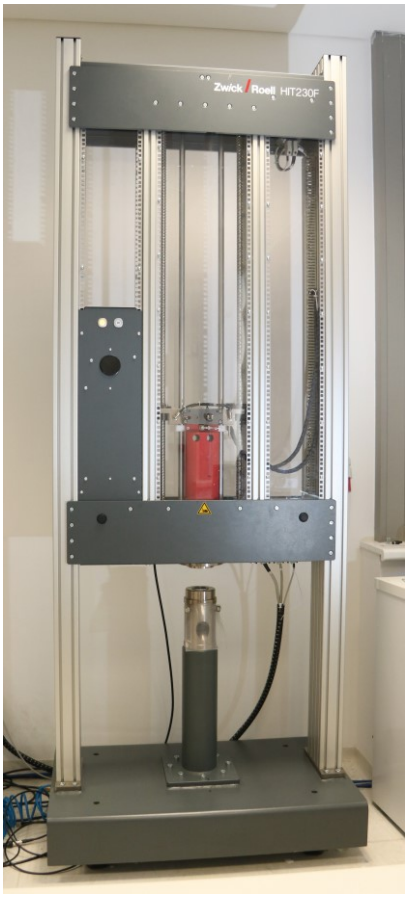

Fig. 1. Drop weight test machine used at Faculty of Applied informatics, TBU Zlin

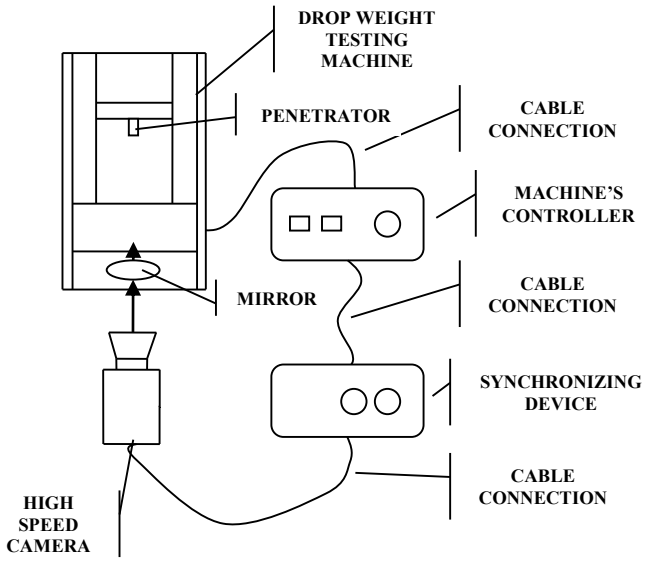

Fig. 2. Arrangement of the measuring station

- What is the origin of the delay? Is it produced by the driver of the drop weight test machine, the synchronizing device or the camera itself?
- Is the delay of a constant value or does it vary in time?
- What are the accurate values of the delay?

The hereby described testing device for validation of synchronization of the high speed camera should help us to receive answers to the above mentioned questions.

III. INITIAL ASSUMPTIONS

Before we designed the hereby described testing device, the following matters of fact have been assumed:

The synchronizing device is quite a simple unit constructed on the basis of combinational and sequential logic gates. Its duty is to generate sharp triggering pulse for the high speed camera in the moment right before the penetrator of the drop weight test machine hits the tested material and to set the length of the triggering pulse according to requirements of the laboratory technician. The length of the trigger pulse determines the length of the record. It is not expected that this device would cause a considerable time delay.

The moment at which the penetrator approaches the tested material is captured by means of an optical gate mounted in its trajectory. The signal generated by the optical gate is then processed by the controlling unit of the drop weight test machine and then it drives the input of the synchronization device.

The producer of the high speed camera does not specify whether there is a delay between the trigger pulse and the start of the recording. However, the high speed camera is the most suspicious of all devices as, concerning its trigger input, there

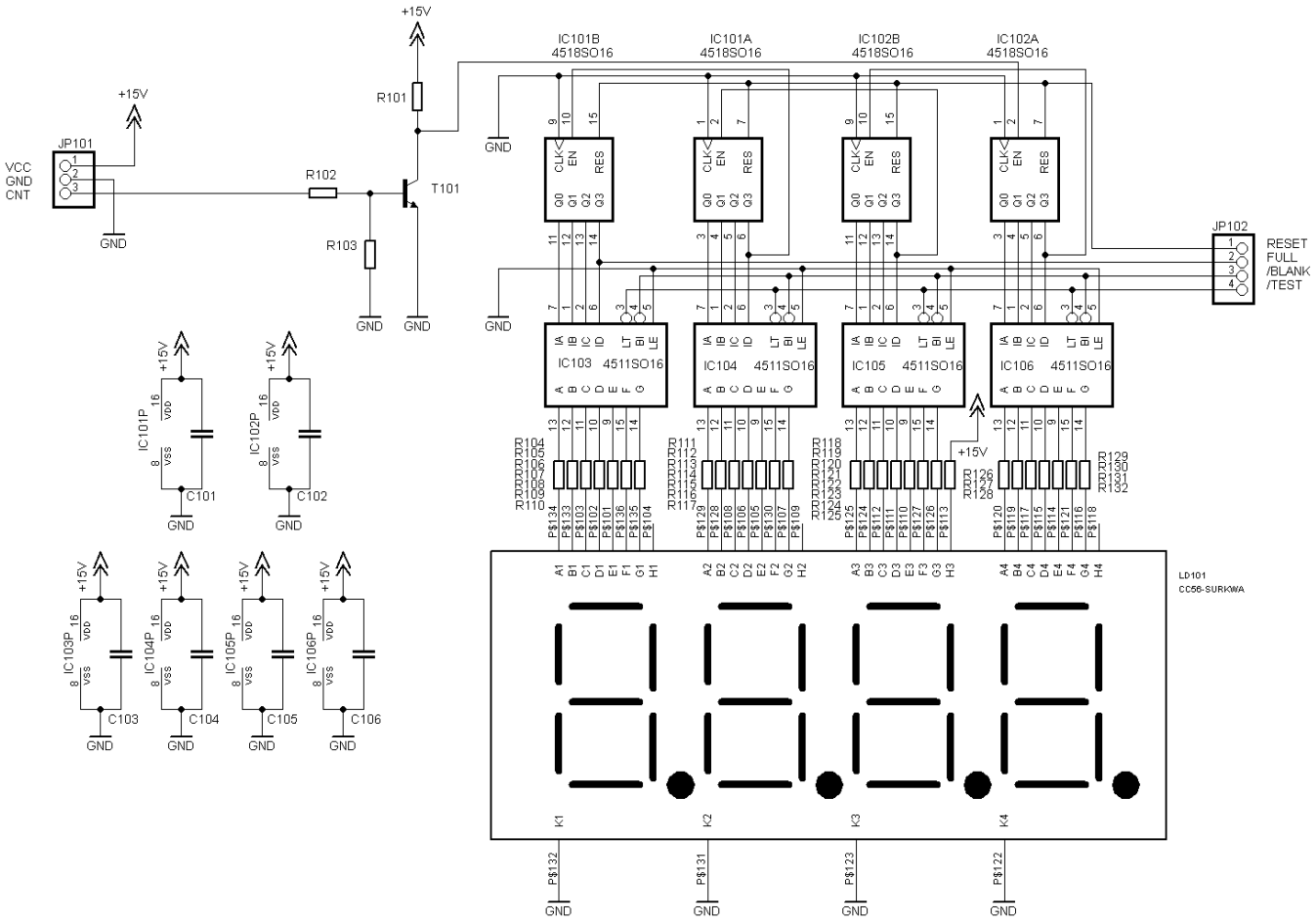

Fig. 3. Connection diagram of the display board

were more rather unclear specifications provided by its manufacturer.

It is obvious that the total delay time T is composed of several components and it can be described by the following equation:

$$T = t_{dd} + t_{ds} + t_{dc}\ [s] \qquad (1)$$

Where:

t_{dd} – delay of the optical gate and the drop weight machine's controller,
t_{ds} – delay of the synchronizing device,
t_{dc} – delay of the camera.

The delay of the synchronizing device t_{ds} can simply be measured by means of an oscilloscope, checking the delay between the input and the output of the circuit when the circuit is driven from a source of pulses. The delay of the optical gate and the drop weight machine t_{dd} is much more complicated to determine. Nevertheless, the delay of the camera t_{dc} can be measured by means of the hereby described device and as the total delay T can be determined from the record captured by the camera, the component t_{dd} may be calculated subsequently.

IV. Testing Device Design

In this chapter, the design of the testing device is described. Although its development was initiated by the above mentioned problems that occurred when we were processing drop weight tests in common with high speed camera records, the device can be used to test the trigger input of all cameras with TTL trigger inputs.

A. Principle of Operation

The principle of operation of the hereby described device is as follows. When a button is pressed, the device generates the trigger pulse immediately and at the same moment it launches an incremental counter that drives a digital display. The displayed value is incremented in the period of 100 µs. When the camera lens is focused on this display, the value captured at the first shot corresponds to the camera's delay. Now the camera's delay t_{dc} is known.

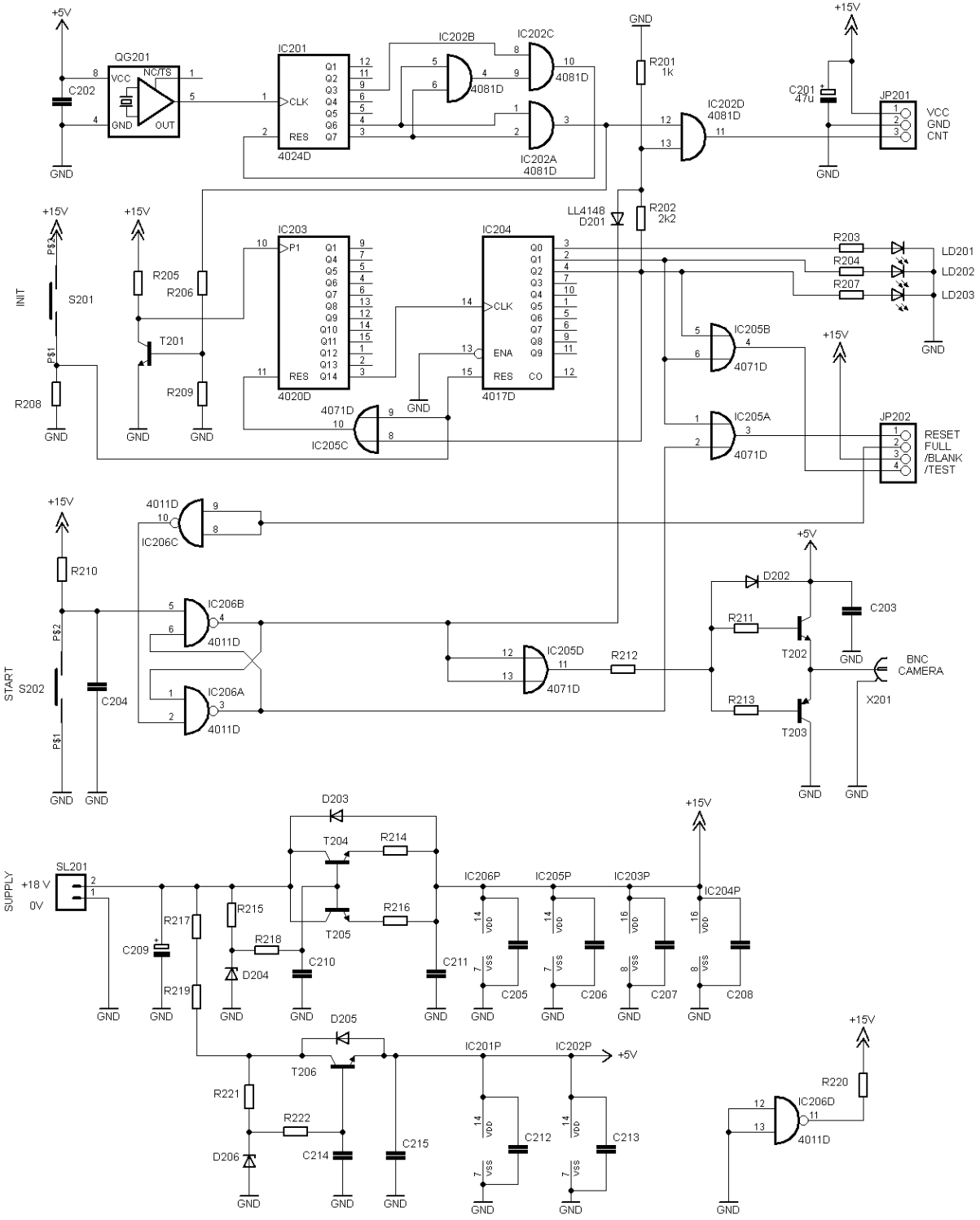

Fig. 4. Connection diagram of the time base board

B. Design Requirements

When designing the circuitry of the testing device the following aspects have been taken into consideration:

1. Display and time base circuits should be constructed separately. This allows us to make changes in the circuitry of the time base, if needed, without the need to construct the whole device.

2. CMOS gates are easy to purchase and nowadays they are still applicable as they provide fast and predictable time response. No microcontroller has been used in this construction.
3. Accurate clock signal must be generated.
4. The higher the supply voltage is the faster is the response of the CMOS gates as well as the response of the display's segments.
5. The camera's input is sensitive to the rising or falling edge of the trigger signal. TTL levels are supported.

C. Design Description

According to the Design Requirements, the testing device for camera's synchronization has been developed. Concerning the requirement 1, it is composed of two separate boards place one above the other. The time base board creates the main board above which the display board is mounted, being connected by means of two connectors. According to the requirement 2, CMOS gates have been used. The main power supply of the device is, concerning the requirement 4, is 15 V. However, concerning the requirements 3 and 5, some parts of the device are supplied by the voltage decreased to 5 V, as the common crystal oscillator power supply voltages are usually 5 V or lower.

1) Display Board

The connection diagram of the display board is depicted in Fig. 3. In fact, the board can operate as a universal counter. Two connectors are used to maintain connection between this board and the time base board. In Fig. 3 these connectors are marked as JP101 and JP102. The meanings of the pin names are enlisted in Table 1.

TABLE I. SIGNALS BETWEEN DISPLAY AND TIME BASE BOARDS

Signal	Description
VCC	Power supply (15 V, 600 mA max.)
GND	Ground
CNT	Count; TTL level, increments on falling edge
RESET	Reset; 15 V level, LOG1 resets counter to 0
FULL	Indicates counter overflow; 15 V level, LOG1 stops counting
$\overline{\text{BLANK}}$	15 V level; LOG0 dims the display
$\overline{\text{TEST}}$	15 V level; LOG0 drives all display segments high

The stated above, the display board is equipped also with an incremental counter which is assembled of two CMOS dual counters IC101 and IC102. The counter increments on falling edge of the driving signal as the input signal is inverted by the level converter consisting of the transistor T101 and the relevant resistors. The level converter is necessary as the clock signal is of TTL level. Once the counter reaches the value of 9999, the FULL signal is generated to stop the time base delivering the CNT (clock) signal. The binary outputs of the counter chips directly drive the inputs of 7 segment display controllers IC103, IC104, IC105 and IC106. The segments of the display LD1 are driven through the current limiting resistors R104 to R132. In order to achieve fast response, the segments are driven by relatively high currents (approximately 20 mA) from the source of the high voltage (the output voltage at the outputs of the appropriate controllers is approximately 13 V). It is worth mentioning that the display is recorded by the high speed camera and therefore the segments cannot be driven in a multiplexed way nor any other type of pulse driving is inadmissible.

As the display is expected to present the time information in [ms] and the CNT signal period is 100 μs, the appropriate decimal point between the 1st and 2nd position from the left side of the display is permanently on.

2) Time Base Board

The time base board drives the display board by means of the signals described in Table 1. It also contains a BNC connector for connecting the camera and the power supply connector. The circuit diagram of the time base board is depicted in Fig. 4.

The required power supply voltage is 18 V. This voltage level is then stabilized to 15 V or 5 V respectively. For this purpose, the Zener diodes D204 and D206 are applied together with the transistors T204, T205 and T206 that serve also as the capacity multipliers. Two transistors T204 and T205 are employed in the 15V branch as the power supply demand of the display is rather high (approximately 600 mA when all segments are on).

The two-level power supply is necessary to comply with the requirements 3 and 4. In order to obtain accurate clock signal, 1 MHz crystal oscillator QG201 has been incorporated. This oscillator requires the power supply voltage as high as 5 V. The clock frequency generated by the oscillator is then divided by 100 in order to achieve the clock period of 100 μs. The divider is based on the counter IC201 and the AND gates IC202A, IC202B and IC202C that generate RESET signal for the counter IC201 each time it reaches the binary number 1100100 (= 100). The gate IC202D then switches the clock signal to the display/counter board. As well as the oscillator QG201, also the devices IC201 and IC202 are fed with the power supply voltage of 5 V. The operation of the circuit was checked by means of SPICE simulation. The length of the falling edge at the transistor T101 is approximately 100 ns.

The board is equipped with two press buttons. The press button S201 (INIT) processes the initialization. It serves as a reset of the whole time base. The initialization is also processed when the circuit is connected to the time base. It consists of three steps. In the first step, $\overline{\text{TEST}}$ signal is generated and LD201 is lit. In the second step, the $\overline{\text{TEST}}$ signal is still generated and it is accomplished with the RESET signal. LD202 is lit. In the third step, both the $\overline{\text{TEST}}$ and RESET signals are deactivated. Now LD203 is lit and the circuit is ready to be used. The gate IC202D would now be unblocked if there was no diode D201. However, the R/S latch circuit is in R state by default until the button S202 (START) is pressed. The timing of the initial phase is assured by the level converter with the transistor T201 and the counters IC203 and IC204. The counter IC203 divides the 10 kHz clock signal by 2^{14}, resulting in the period of approximately 1.6 s. Each 1.6 s the Johnson's counter IC204 increases its output state until the third step is reached. Then the counter IC203 is blocked by the RESET signal, passing through the gate IC205C. The

initialization can be repeated by pressing the button S201 (INIT) that causes reset of the counter IC204.

Once the initialization is finished and LD203 is lit, the circuit waits until the button S202 (START) is pressed. Then the R/S latch circuit switches to the S state and now the gate IC202D is definitely unblocked. Because the counter on the display board was reset during the initialization, it starts to count from 0 to 999.9 ms. At the same moment the high TTL level occurs at the trigger output X201. Once the value of 999.9 is reached, the counter generates FULL signal that switches the appropriate R/S latch circuit to the R state. By pressing the button S202 again, the above described cycle is repeated.

The selection of the crystal is not critical, as a typical low-cost crystal with the accuracy of 100 ppm provides the measurement uncertainty of 0.01 %.

V. CONCLUSIONS

In this paper a method of synchronizing a high speed camera with drop weight test machine is briefly described as well as its advantages and disadvantages. Because there is a need to determine the delay between the time when the camera obtained the trigger pulse and the time when the camera started recording, the hereby described testing device has been developed. The device allows the operator to measure the camera's delay in the range from 1 to 999 ms with the step of 0.1 ms.

Unfortunately, due to procedural delays, at the time of submission of this manuscript, the construction of the device was not fully tested for the proper operation. Therefore the authors cannot provide information on the accuracy of the results obtained by the device. However, first tests have been performed, showing that the camera's delay with the t_{dc} of approximately 10 ms is prevailing in the total delay time T.

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