# Voltage Balancing in Five-Level Diode-Clamped Power Converters\*

Francisco Umbría \* Fabio Gómez-Estern \* Francisco Gordillo \* Francisco Salas \*

\* Department of Systems Engineering and Automation, University of Seville, 41092 Seville, Spain (e-mail: fumbria@us.es, gordillo@etsi.us.es, fabio@esi.us.es, salas@cartuja.us.es)

Abstract: This paper addresses the voltage imbalance problem of the dc-link capacitors in multilevel power converters. Considering the five-level diode-clamped converter, a mathematical analysis of the capacitor voltage difference dynamics is carried out. It leads to a new problem statement that relates the voltage balancing objective to a problem of ensuring the practical stability of a nonlinear system in the presence of disturbances. Then, exploiting the properties and knowledge of the disturbance patterns, a novel and simple controller is presented. Simulation results are included to validate the performance of the proposed controller.

#### 1. INTRODUCTION

Since the topology of the diode-clamped converter (DCC), also known as neutral-point-clamped converter, was proposed in the early 80's by Nabae et al. [1981], multilevel power converters are being increasingly employed in the industry, mainly in high-power applications (Kouro et al. [2010]). Bi-directional power flow, near sinusoidal currents and high efficiency are some of the attractive features that these power conversion systems present.

Each phase of a multilevel converter can generate more that two different voltage levels. Thus, compared with the conventional two-level converter, the generated voltages have more possible steps to approach the sinusoidal waveforms, reducing in this way the harmonic distortion (Rodríguez et al. [2009]). Nevertheless, the increase of the number of voltage levels leads to a higher complexity of the converter structure. Moreover, additional dc-link capacitors are also required in some topologies such as the DCC. Concerning these capacitors, the balancing of their voltages according to an operating point is one of the mayor technical challenges of the multilevel converters.

The phenomenon of the dc-link capacitor voltage imbalance, besides deteriorating the performance of the system, can even cause the operational failure of the converter. Focusing on the five-level DCC, topology considered in this paper and illustrated in Fig. 1, the capacitor voltages tend to rise or fall in an uncontrolled way due to the different capacitor charging times during instantaneous active power transfers. Besides, considering conventional modulation techniques, this converter presents some theoretical and practical limits (Marchesoni and Tenca [2001], Saeedifard et al. [2007]), for which an equal capacitor voltage sharing is not possible in all the operating conditions.

To overcome the problem, several approaches have been considered in the last years. Most of them include addi-

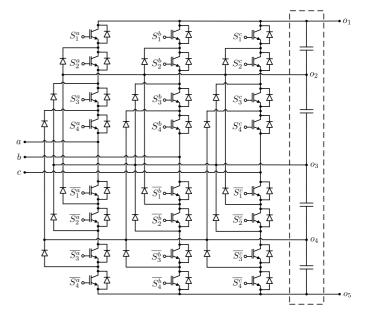


Fig. 1. Circuit of a five-level diode-clamped converter.

tional power hardware (Shu et al. [2013], Shukla et al. [2008]), representing a significant increase in the converter cost. Others are based on the use of non-conventional modulation strategies to guarantee the capacitor voltage balancing (Saeedifard et al. [2009], Busquets-Monge et al. [2008]) and require higher computational time.

This paper studies the voltage imbalance problem, based on a model of the five-level DCC, carrying out a mathematical analysis of the capacitor voltage difference dynamics. Considering some practical assumptions, the analysis leads to an approximated model that contains several sinusoidal functions of time. These functions are treated as periodic disturbances produced by some external generator. In this manner, it is shown that the problem of the capacitor voltage imbalance can be addressed as a problem of ensuring the regulation of the variables of a nonlinear system subject to exogenous disturbances. Then,

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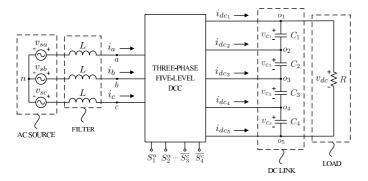


Fig. 2. Schematic diagram of the five-level diode-clamped converter working as a rectifier.

a novel voltage balance controller based on the preliminary analysis worked out is presented. The salient feature of the proposed controller is that it enables voltage balancing with no requirements for auxiliary circuitry, and with reduced computational cost as well.

The outline of the paper is the following. In Section 2, the model of the five-level DCC is described. Afterwards, the control objective addressed in this paper is stated in Section 3. Section 4 is devoted to the analysis of the converter dynamics, while the design and implementation of the proposed controller is shown in Section 5. The simulation results obtained applying the proposed control law are discussed in Section 6. Finally, some conclusions are drawn in Section 7.

#### 2. MODEL OF THE CONVERTER

The rectifier operation mode of the five-level DCC is the setup considered in this paper. Figure 2 shows a schematic diagram of this configuration, whose primary application is to derive dc power from an ac source or from the grid. The dc link is composed of capacitors  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$ , all of identical capacitance C. Their voltages are represented by  $v_{c_1}$ ,  $v_{c_2}$ ,  $v_{c_3}$  and  $v_{c_4}$ , respectively. The phase currents are denoted by  $i_a$ ,  $i_b$  and  $i_c$ , and the phase voltages are defined by  $v_{sa}$ ,  $v_{sb}$  and  $v_{sc}$ .

In order to describe the converter dynamics, the model of the DCC presented in Portillo et al. [2005] is adopted. This model describes, in  $\alpha\beta\gamma$  orthogonal coordinates, the dynamics of the phase currents and of the total dc-link voltage, as well as those of the dc-link capacitor voltage differences. For this purpose, the voltage differences

$$v_{d_1} = v_{c_1} - v_{c_4} \tag{1}$$

$$v_{d_2} = v_{c_2} - v_{c_3} (2)$$

$$v_{d_3} = v_{c_3} - v_{c_4}, (3)$$

are introduced in the modeling process. Notice that, in this continuous model, the control inputs are defined by  $\delta_{\alpha}$ ,  $\delta_{\beta}$  and  $\delta_{\gamma}$ . They represent the averaged values in a switching period of the gating signals of the converter power switches. In addition, the phase currents are transformed into  $i_{\alpha}$  and  $i_{\beta}$ , and the phase voltages into  $v_{\alpha}$  and  $v_{\beta}$ .

Focusing on the variation over the time of the voltage difference variables, when some terms present in the model are grouped, the following expressions are derived

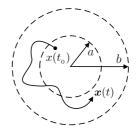


Fig. 3. Practically stable system with respect to parameters a and b.

$$C\frac{dv_{d_1}}{dt} = g_{13} \,\delta_{\gamma}^3 + g_{12} \,\delta_{\gamma}^2 + g_{11} \,\delta_{\gamma} + g_{10} \tag{4}$$

$$C\frac{dv_{d_2}}{dt} = g_{23} \,\delta_{\gamma}^3 + g_{22} \,\delta_{\gamma}^2 + g_{21} \,\delta_{\gamma} + g_{20} \tag{5}$$

$$C \frac{dv_{d_3}}{dt} = g_{33} \,\delta_{\gamma}^3 + g_{32} \,\delta_{\gamma}^2 + g_{31} \,\delta_{\gamma} + g_{30}, \qquad (6)$$

where  $g_{ij}$  for i=1, 2, 3, and j=0, 1, 2, 3, are nonlinear functions. These complicated functions depend on the phase currents and on the control inputs  $\delta_{\alpha}$  and  $\delta_{\beta}$ . Therefore,

$$g_{ij} = g_{ij}(i_{\alpha}, i_{\beta}, \delta_{\alpha}, \delta_{\beta}),$$
 (7)

for  $i=1,\,2,\,3,$  and  $j=0,\,1,\,2,\,3.$  The exact expressions of these functions can be consulted in Portillo et al. [2005] and are omitted in this paper for brevity.

## 3. CONTROL OBJECTIVE: PRACTICAL STABILITY

With the purpose of coping with the voltage imbalance problem of the dc-link capacitors, the following control objective defined in relation to the voltage difference variables (1)-(3) is stated:

1. The voltage difference variables  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$  should be regulated to avoid the uncontrolled rise or fall of the dc-link capacitor voltages.

This control objective is related to the practical stability of the system, concept introduced by Lasalle and Lefschetz [1961] and also referred to as ultimate boundedness. Note that the control objective can be addressed as a problem of assuring that the response of the system to given stimuli is contained within certain specified bounds. In other words, variables  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$  should be controlled, remaining within a domain defined by a ball centered at zero,  $\forall t$ .

Definition 1. A system is said to be practically stable if there exist positive constants b and c, independent of  $t_0 \geq 0$ , and for every  $a \in (0, c)$ , there is  $T_{ab} = T_{ab}(a, b) \geq 0$ , independent of  $t_0$ , such that

$$||x(t_0)|| \le a \implies ||x(t)|| \le b, \qquad \forall t \ge t_0 + T_{ab}, \quad (8)$$

where  $x \in \mathbb{R}^n$  is the state of the system. Figure 3 illustrates this type of stability in terms of trajectory behavior.

Nonetheless, other control requirements of the system should be also fulfilled. Thereby, the instantaneous active and reactive powers, denoted by p and q, respectively, and defined in a three-phase circuit by

$$p = v_{\alpha}i_{\alpha} + v_{\beta}i_{\beta} \tag{9}$$

$$q = v_{\alpha}i_{\beta} - v_{\beta}i_{\alpha}, \tag{10}$$

should track their references, described by  $p^*$  and  $q^*$ . Besides, the total dc-link voltage, denoted by  $v_{dc}$ , should be regulated towards the constant reference  $v_{dc}^*$ .

In the rest of the paper it is assumed that there exist certain controllers that deal with the regulation of the instantaneous powers and of the total dc-link voltage. Specifically, the control inputs  $\delta_{\alpha}$  and  $\delta_{\beta}$  as well as  $p^*$  are used by these controllers to this end.

# 4. ANALYSIS OF THE DYNAMICS OF THE DC-LINK CAPACITOR VOLTAGE DIFFERENCES

This section is devoted to study the system (4)-(6), analyzing in detail functions (7), in order to provide a better understanding of the behavior of the DCC. The following assumptions are considered in the analysis.

Assumption 1. The instantaneous power dynamics are much faster than both total dc-link voltage and capacitor voltage difference dynamics.

This assumption is related to an approach based on different time scales and leads to consider in the analysis that the instantaneous powers have been regulated around their references, that is,

$$p \simeq p^* \tag{11}$$

$$q \simeq q^*. \tag{12}$$

Assumption 2. The total dc-link voltage has been properly regulated and can be approximated by its steady-state reference as follows

$$v_{dc} \simeq v_{dc}^*.$$
 (13)

Under this assumption, it is supposed that after certain period of time the total dc-link voltage  $v_{dc}$  has achieved its reference, regardless of the behavior of the variables  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$ . In this way, it is also assumed that the capacitor voltage differences are bounded, so during the transient state of  $v_{dc}$  the trajectories of  $v_{d_1}$   $v_{d_2}$  and  $v_{d_3}$  have not escaped to infinity. It is important to mention that when  $v_{dc}$  has achieved its reference, the instantaneous active power reference can be approximated by

$$p^* \simeq \frac{v_{dc}^{*^2}}{R}.\tag{14}$$

Summarizing, when these assumptions are taken into account, it leads to study functions (7) focusing on a specific operating point of the system, which is defined by the references  $p^*$ ,  $q^*$  and  $v^*_{dc}$ .

The procedure to deduce the final expressions of (7) is similar to the one presented in Umbría et al. [2009] for the three-level DCC and leads to define the functions

$$\omega_{ij}(t) = g_{ij}|_{ss} \simeq \mu_{ij}\sin(3\cdot 2\pi ft + \theta_{ij}) + \eta_{ij}, \quad (15)$$

for i=1,2,3, and j=0,1,2,3. The subscript ss indicates the condition of steady state of the system. Parameters  $\mu_{ij}$ 

Table 1. Parameters of the study system.

Parameter	Value
Total dc-link voltage reference $(v_{dc}^*)$	700 V
Instantaneous reactive power reference $(q^*)$	$0~\mathrm{VAr}$
Ac-source frequency $(f)$	$50~\mathrm{Hz}$
Phase voltages $(v_{sa}, v_{sb}, v_{sc})$	$230~\mathrm{V_{RMS}}$
Inductors $(L)$	3  mH
Capacitors $(C_1, C_2, C_3, C_4)$	$4700~\mu\mathrm{F}$
Resistive load $(R)$	120 $\Omega$

and  $\theta_{ij}$  are the amplitudes and phases of the sinusoidal terms of functions  $\omega_{ij}(t)$ , and  $\eta_{ij}$  are their mean values. They all depend on the particular values of  $p^*$ ,  $q^*$  and  $v_{dc}^*$ . Furthermore, the frequency of the sinusoidal terms of functions  $\omega_{ij}(t)$  corresponds with the triple frequency of the ac-source frequency, denoted by f, which is also the frequency of the phase voltages.

As a result, introducing in (4)-(6) the practical assumptions considered, and assuming that the dc-link capacitor voltage differences are close to zero, the dynamics of  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$  can be expressed as

$$C \frac{dv_{d_1}}{dt} = \omega_{13}(t) \,\delta_{\gamma}^3 + \omega_{12}(t) \,\delta_{\gamma}^2 + \omega_{11}(t) \,\delta_{\gamma} + \omega_{10}(t) \tag{16}$$

$$C \frac{dv_{d_2}}{dt} = \omega_{23}(t) \,\delta_{\gamma}^3 + \omega_{22}(t) \,\delta_{\gamma}^2 + \omega_{21}(t) \,\delta_{\gamma} + \omega_{20}(t) \tag{17}$$

$$C \frac{dv_{d_3}}{dt} = \omega_{33}(t) \,\delta_{\gamma}^3 + \omega_{32}(t) \,\delta_{\gamma}^2 + \omega_{31}(t) \,\delta_{\gamma} + \omega_{30}(t),$$
 (18)

where  $\delta_{\gamma}$  is the control input of the system. Notice that the dynamics of the state variables  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$  of this approximated model are decoupled.

Application example 1. Consider the values of the system parameters shown in Table 1. Note that the instantaneous reactive power reference is set to zero in order to achieve unity power factor, and that the steady-state reference of the instantaneous active power can be approximated by (14). In this specific operating point, the behavior of functions (15) is depicted in Fig. 4. Most of these functions present a sinusoidal behavior, having they all the same frequency, while the rest are constant functions.

Remark 1. The analysis has resulted in an approximated model (16)-(18), which presents only the control input  $\delta_{\gamma}$  to regulate the variables  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$ , whose dynamics are decoupled. Besides, the system of equations (16)-(18) is not controllable. For instance, given an initial state of  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$ , these variables can not be driven to some other state and being kept indefinitely in the new state. To see this, notice that  $\delta_{\gamma}$  can not be defined to provide a solution to  $\dot{v}_{d_1} = 0$ ,  $\dot{v}_{d_2} = 0$  and  $\dot{v}_{d_3} = 0$  at the same time. Hence, guaranteeing the asymptotic stability of the origin of the system is not possible, and the practical stability of the system is consequently the purposed control objective.

The approximated model contains also several sinusoidal functions of time, which are defined by (15). In what follows, these functions are assumed to be external disturbances. In this way, the cardinal results obtained in

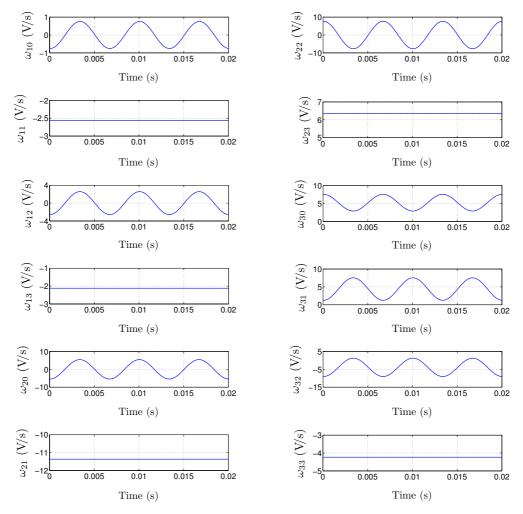


Fig. 4. Functions  $\omega_{ij}(t)$  for i=1, 2, 3, and j=0, 1, 2, 3, considering the parameters of Table 1.

this section lead to relate the capacitor voltage balancing objective to a problem of ensuring the practical stability of the variables of the nonlinear system (16)-(18) subject to known exogenous disturbances (15). This novel problem statement is considered in this paper to design the voltage balance controller, making use of the special features of the disturbances.

#### 5. CONTROLLER DESIGN AND IMPLEMENTATION

In order to practically stabilize the voltage difference variables, the proposed control law to apply at certain sampling instant  $t_o$  is described by

$$\delta_{\gamma} = \begin{cases} \delta_{\gamma_{1}}, & \text{if } \omega_{31}(t) \leq \rho \text{ and } t_{o} \leq t < t_{o} + T \\ \delta_{\gamma_{2}}, & \text{if } \omega_{31}(t) > \rho \text{ and } t_{o} \leq t < t_{o} + T, \end{cases}$$
(19)

where T is the period defined by

$$T = \frac{1}{3f} = t_{\gamma_1} + t_{\gamma_2}. \tag{20}$$

Constant  $\rho$  is a design parameter, and  $\delta_{\gamma_1}$  and  $\delta_{\gamma_2}$  are constant values to be chosen. It is worth stressing that T is defined to coincide with the period of the sinusoidal terms of the disturbances (15), which is known. The total time

intervals when the values  $\delta_{\gamma_1}$  and  $\delta_{\gamma_2}$  are applied during a period are defined, respectively, by  $t_{\gamma_1}$  and  $t_{\gamma_2}$ . With the aim of implementing this control law, which is focused on a particular system operating point given by  $p^*$ ,  $q^*$  and  $v_{dc}^*$ , several off-line steps should be carried out.

Remark 2. The motivation for the control law is the following. There exists an only control input to deal with three variables with decoupled dynamics (16)-(18). It suggests to use  $\delta_{\gamma}$  to control any variable (of some of them) during some periods of time and to use it to control the rest of the variables (or the remaining one) in the spare time. As can be seen in (19), the selection of the control values to apply in each time instant is based on the evaluation of  $\omega_{31}(t)$ . This choice is motivated by the fact that, when  $\delta_{\gamma}$  is small,  $\omega_{31}(t)$  multiples  $\delta_{\gamma}$  in (18), and this term is the  $\delta_{\gamma}$ -dependent dominant term of the equation. Notice that the corresponding terms in (16) and (17), that is, the disturbances  $\omega_{11}(t)$  and  $\omega_{21}(t)$ , are constants. In view of this, it is reasonable to control  $v_{d_3}$  when  $\omega_{31}$  is large and control the other variables when the contrary occurs.

#### 5.1 Voltage difference variations during a period T

In the first controller design step, the net variation of  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$  during a period T, based on the application of (19), is analyzed as a function of  $\delta_{\gamma_1}$  and  $\delta_{\gamma_2}$ .

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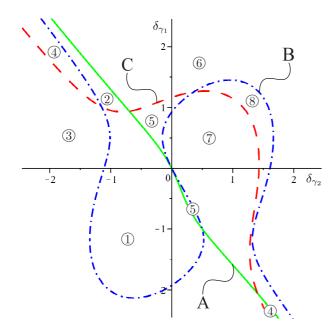


Fig. 5. Areas in the control input space  $\delta_{\gamma_2}$ –  $\delta_{\gamma_1}$  delimited by the curves  $\Delta v_{d_i}|_{t_o}^{t_o+T}=0$  for  $i=1,\,2,\,3$ , which are denoted, respectively, by A, B and C.

Integrating first (16) and (17) from  $t_o$  to  $t_o + T$ , it yields the expressions

$$\Delta v_{d_i}\big|_{t_o}^{t_o+T} = \eta_{i3} \left( t_{\gamma_1} \delta_{\gamma_1}^3 + t_{\gamma_2} \delta_{\gamma_2}^3 \right) + \frac{\left(-1\right)^i \mu_{i2}}{3 \cdot 2\pi f} \lambda \left( \delta_{\gamma_1}^2 - \delta_{\gamma_2}^2 \right) + \eta_{i1} \left( t_{\gamma_1} \delta_{\gamma_1} + t_{\gamma_2} \delta_{\gamma_2} \right), \tag{21}$$

for i=1, 2. Parameter  $\lambda$  is a positive constant that depends on the specific value of  $\rho$  (defined in (19)) chosen. For the variable  $v_{d_3}$ , the equation obtained by integrating (18) is described by

$$\Delta v_{d_3} \Big|_{t_o}^{t_o+T} = \eta_{33} \left( t_{\gamma_1} \delta_{\gamma_1}^3 + t_{\gamma_2} \delta_{\gamma_2}^3 \right) + \eta_{32} \left( t_{\gamma_1} \delta_{\gamma_1}^2 + t_{\gamma_2} \delta_{\gamma_2}^2 \right)$$

$$+ \frac{\mu_{32} \lambda}{3 \cdot 2\pi f} \left( \delta_{\gamma_2}^2 - \delta_{\gamma_1}^2 \right) + \eta_{31} \left( t_{\gamma_1} \delta_{\gamma_1} + t_{\gamma_2} \delta_{\gamma_2} \right)$$

$$+ \frac{\mu_{31} \lambda}{3 \cdot 2\pi f} \left( \delta_{\gamma_2} - \delta_{\gamma_1} \right) + \eta_{30} T .$$
(22)

Then, these expressions are solved for the particular situation  $\triangle v_{d_i}|_{t_o}^{t_o+T}=0$  for  $i=1,\,2,\,3$ . Thereby, the pairs of control values  $\delta_{\gamma_1}$  and  $\delta_{\gamma_2}$  that make that the variation of the dc-link capacitor voltage differences remains constant during a specific period T, defined by (20) and identical to the period of the sinusoidal terms of the disturbances (15), are computed.

Application example 2. Consider the values of the system parameters shown in Table 1 that lead to the behavior of the disturbances (15) depicted in Fig. 4. Selecting parameter  $\rho$  of (19) in such a way that time intervals  $t_{\gamma_1}$  and  $t_{\gamma_2}$  are set as

$$t_{\gamma_1} = \frac{T}{3}, \qquad t_{\gamma_2} = \frac{2T}{3},$$
 (23)

Table 2. Description of the areas defined in the control input space  $\delta_{\gamma_2} - \delta_{\gamma_1}$ .

	$\triangle v_{d_1}\Big _{t_o}^{t_o+T}$	$\triangle v_{d_2}\Big _{t_o}^{t_o+T}$	$\triangle v_{d_3}\Big _{t_o}^{t_o+T}$
Area 1	+	+	+
Area 2	+	+	_
Area 3	+	_	+
Area 4	+	_	_
${\rm Area}\ 5$	_	+	+
Area 6	_	+	_
Area 7	_	_	+
Area 8	_	_	_

the curves in the control input space  $\delta_{\gamma_2} - \delta_{\gamma_1}$  that satisfy the expressions  $\Delta v_{d_i}|_{t_o}^{t_o+T} = 0$  for i=1, 2, 3, are illustrated in Fig. 5, denoted by A, B and C, respectively. These three curves delimit certain areas in the control input space, which are numbered from one to eight in the figure. According to Table 2, the selection of a couple of values  $\delta_{\gamma_1}$  and  $\delta_{\gamma_2}$  in a particular area causes distinct effect in the variables  $\Delta v_{d_i}|_{t_o}^{t_o+T}$  for i=1,2,3, since the areas are based on a partition of the control input space such that each subset provides a different set of signs of these variables.

# 5.2 Generation of the look-up table for $\delta_{\gamma}$

In this last off-line step, a look-up table for control input  $\delta_{\gamma}$  is created. This table consists of a set of couples of control values  $\delta_{\gamma_1}$  and  $\delta_{\gamma_2}$  and is created selecting a particular pair of values for each one of the eight areas described in Table 2, resulting of solving expressions (21) and (22).

#### 5.3 Implementation of the control law

The implementation of the control law is simple and presents lower computational cost than other voltage balancing strategies. It is based on the on-line evaluation of the signs of the variables  $v_{d_1}, \ v_{d_2}$  and  $v_{d_3}$  each certain sampling period T (20), which is equal to the period of the sinusoidal terms of the disturbances (15). Depending on the signs of these three variables, the specific couple  $\delta_{\gamma_1}$  and  $\delta_{\gamma_2}$  of the look-up table that produces the opposite effect to that marked by the signs of  $v_{d_1}, \ v_{d_2}$  and  $v_{d_3}$  in the variables  $\Delta v_{d_i}|_{t_o}^{t_o+T}$  for i=1,2,3, is selected. Then, control law (19) is applied. The process is repeated each sampling period of time.

### 6. SIMULATION RESULTS

The evaluation results of the five-level DCC usefulness under the proposed voltage balancing strategy are shown in this section. For this purpose, the equations that describe the converter dynamics (Portillo et al. [2005]) together with the voltage balance controller have been implemented in Simulink under MATLAB environment, carrying out a simulation in discrete time with sampling time set to 200  $\mu$ s. The controllers presented in Vázquez et al. [2008] have been also included in the system with the goal of

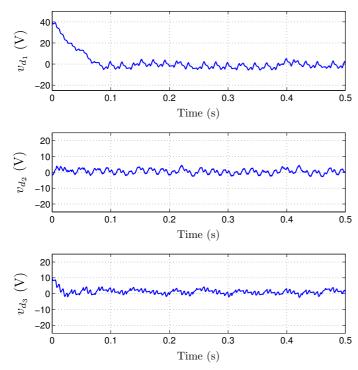


Fig. 6. Behavior of the dc-link capacitor voltage differences under the proposed controller.

regulating the instantaneous powers and the total dc-link voltage. The values of the system parameters considered are summarized in Table 1. Notice that the sampling time is lower than the period (20) of the sinusoidal terms of the disturbances (15), used to determine when should the signs of the variables  $v_{d_1}$ ,  $v_{d_2}$  and  $v_{d_3}$  be evaluated. It is important to note that the simulation is directly based on the continuous model of the five-level DCC, so no switching strategy is required.

The behavior of the system have been studied for a particular operating point, starting the simulation with unequal values of the dc-link capacitor voltages. This operation point is defined by the references  $v_{dc}^*$  and  $q^*$  described in Table 1, and also by the value of  $p^*$  in steady state, which is approximated by (14). Thus, the couples of values of the look-up table for  $\delta_{\gamma}$  have been off-line calculated for these specific conditions of operation.

Figure 6 depicts the evolution of the dc-link capacitor voltage differences. The variables  $v_{d_1}$  and  $v_{d_3}$  move rapidly to zero, remaining fluctuating, together with  $v_{d_2}$ , around this value. After approximately 0.1 s, the voltage differences satisfy the condition  $|v_{d_i}(t)| \leq 5$  V, for i=1,2,3. Hence, from that moment onwards, the three state variables are kept close to zero, as it is required. Therefore, the proposed controller presents a satisfactory performance, since it avoids the uncontrolled rise of fall of the capacitor voltages.

# 7. CONCLUSIONS AND FUTURE WORK

This paper has coped with the voltage imbalance problem of the dc-link capacitors in the five-level DCC, introducing a voltage balance controller for a specific operating point of the system. The controller design has been based on the analysis of the converter model dynamics. Simulation results have illustrated the usefulness of the controller.

It should be stressed that the control law, implemented in the converter working as rectifier, can be also used for the inverter mode. In addition, it is extensible, including some non-obvious adjustments, to the back-to-back DCC topology. This is the future direction of research of the authors of this work, together with the extension of the controller to be used under varying operating conditions of the system.

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