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A General Form for Reset Control Including Fractional Order Dynamics ⋆

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Abstract: Currently, reset control focuses on using structures which allow new resetting rules in order to avoid limit cycle to be caused and improve the performance of the system. This paper investigates the properties of some reset strategies, of integer and fractional order, which reset controller states to fixed or variable non-zero values and are able to eliminate or reduce the overshoot in first and higher order systems, respectively. Based on them, a general reset control strategy with fractional order dynamics is proposed with both fixed and variable resetting to non-zero values. A comparative study is given to show its benefits in terms of prevention of limit cycle and reduction of the overshoot. As a result, some guidelines to be considered for the design of such controllers depending on the application are offered.

Keywords: Reset control systems, Limit cycle, Fractional calculus, Feedforward control

1. INTRODUCTION

Since the first reset strategy, the well-known Clegg integrator (CI) (Clegg [1958]), further controllers have been developed to overcome the fundamentals limitations of linear controllers and give more flexibility in controller design. Indeed, correctly designed, the reset action commonly leads to a faster system response without output excessive overshoot, but unfortunately additional negative phenomena may be derived.

Recently, it has been shown that resetting to zero at the zero crossings of the error is completely inadequate since it may cause limit cycle in the system response (see e.g. Baños and Barreiro [2012] and references therein). As a result, current trends in the field focus on using new reset structures which allow reset to occur on more complicated and sophisticated sets so as to improve the performance of the system. To this end, several solutions have been reported in the literature. For example, the controller states were reset to certain non-zero values in Zheng et al. [2007, 2008] to make the system response be even faster in comparison with the linear solution. In Baños and Barreiro [2012], Baños and Vidal [2012, 2007], a PI+CI controller was used to reduce considerably both the percentage of overshoot and the settling time by resetting only a percentage of the integral term of the PI controller. Nesic et al. [2011] proposed a new class of first order reset element (FORE) together with set-point regulation, which allow new resetting rules. And a modified version of this reset strategy was applied in Panni et al. [2012] to a diesel engine. In our previous works (HosseinNia et al. [2013a,b]), the possibilities of using fractional order CI (CI$^\alpha$) with a classic PI controller as base controller were investigated. It was demonstrated that CI$^\alpha$ is also capable of handling the mentioned problems in reset control by adjusting its order adequately.

Given this context, the main objective of this paper is to continue the investigation on different resetting rules. Hence, we summarize the particular properties of different reset controllers, of integer and fractional order, to improve the performance of a system, especially in terms of prevention of limit cycle and traditional time domain specifications. Based on them, a general reset control is proposed. Thus, the contribution of this paper is twofold: (i) propose a general reset structure which will combine some properties of the reviewed reset controllers, and (ii) provide a comparative study and some guidelines for designing such controllers depending on the application.

The remaining of the paper is organized as follows. Section 2 concerns fundamentals of some reset controllers which avoid limit cycle occurrence. Section 3 presents a general reset control strategy which combines features of the previous controllers. A comparative study between the proposed and existing reset strategies is given in Section 4. Finally, Section 5 draws the main conclusions of this paper.

2. MODIFIED RESET CONTROL

This section recalls the formulations and main properties of different reset controllers with zero crossing and periodic reset reported in the literature to avoid the occurrence of limit cycle. In particular, the following reset strategies will be summarized next: (i) reset control based on resetting to a non-zero value periodically, at fixed instants t_k; (ii) a combination of a linear PI and reset –referred to as PI+CI–; (iii) a FORE controller with set-point regulation; (iv) a fractional order version of classical CI with proportional action; and (v) the fractional order ver-

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sion of PI+CI compensator –referred to as PI$^\alpha$+CI$^\alpha$. The latter controller is used in this work to show the possibilities of introducing one more parameter, the order α, to PI+CI compensator.

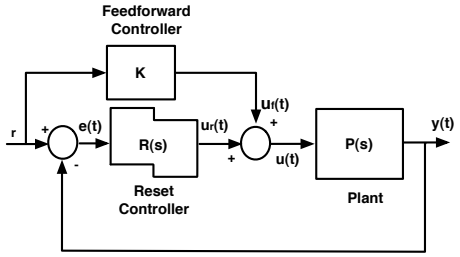

Fig. 1. Block diagram of a reset control system

Basically, the block diagram of a reset control is shown in Fig. 1. In a general form and assuming $K = 0$, the dynamics of a fractional order reset controller can be described by a differential inclusion (DI) as follows:

$$\begin{aligned} D^{\alpha_1} x_r(t) &= A_r x_r(t) + B_r e(t),\ e(t) \neq 0, \\ x_r(t^+) &= A_{R_r} x_r(t),\ e(t) = 0, \\ u_r(t) &= C_r x_r(t) + D_r e(t), \end{aligned} \tag{1}$$

where $\alpha_1 \in \mathbb{R}^+$ is the (fractional) order of the derivative –in the case of an integer order controller: $\alpha_1 = 1$–, matrix $A_{R_r} \in \mathbb{R}^{n_r \times n_r}$, $x_r(t) \in \mathbb{R}^{nr}$ is the reset controller state and $u_r(t) \in \mathbb{R}$ is its output. Let consider a fractional order plant $P(s)$, in general, with the following state space representation:

$$\begin{aligned} D^{\alpha_2} x_p(t) &= A_p x_p(t) + B_p u_r(t), \\ y(t) &= C_p x_p(t), \end{aligned} \tag{2}$$

where $\alpha_2 \in \mathbb{R}^+$ is the basic order of the plant, $A_p \in \mathbb{R}^{n_p \times n_p}$, $B_p \in \mathbb{R}^{n_p \times 1}$, $C_p \in \mathbb{R}^{1 \times n_p}$ are its state, input and output matrices. Assuming $\alpha = \alpha_1 = \alpha_2$, the closed-loop reset control system can be then described by the following DI:

$$\begin{aligned} D^{\alpha} x(t) &= A_{cl} x(t) + B_{cl} r(t),\ x(t) \notin \mathscr{M},\ x(0) = x_0 \\ x(t^+) &= A_R x(t),\ x(t) \in \mathscr{M}, \\ y(t) &= C_{cl} x(t), \end{aligned} \tag{3}$$

where $x = \begin{bmatrix} x_p \\ x_r \end{bmatrix}$, $A_{cl} = \begin{bmatrix} A_p - B_p D_r C_p & B_p C_r \\ -B_r C_p & A_r \end{bmatrix}$, $A_R = \begin{bmatrix} I_{n_p} & 0 \\ 0 & A_{R_r} \end{bmatrix}$, $B_{cl} = [B_p D_r \ \ B_r]^T$, $C_{cl} = [C_p \ \ 0]$. The reset surface $\mathscr{M}$ is defined by $\mathscr{M} = \{x \in \mathbb{R}^n : C_{cl} x = r,\ (I - A_R)x \neq 0\}$, with $n = n_r + n_p$.

In the incommensurate case, i.e., $\alpha_1 \neq \alpha_2$, it is worth remarking that the closed-loop system needs to be augmented to a commensurate system of order $\alpha = \frac{1}{M}$ as follows: writing both the system and the controller orders as $\alpha_i = v_i/u_i$, for $i = 1, 2$, with $(u_i, v_i) = 1$, $u_i, v_i \in \mathbb{Z}^+$, M will be the lowest common multiple of the denominators u_i. Refer to HosseinNia et al. [2010] for more details about augmented systems.

2.1 Controller based on fixed reset instants

Zheng et al. [2007, 2008] proposed a reset controller based on time whose states are reset to certain non-zero values at every instant t_k and makes the system response be faster that the linear solution. It can be represented as follows:

$$\begin{aligned} \dot{x}_r(t) &= A_r x_r(t) + B_r e(t),\ t \neq t_k \\ x_r(t^+) &= E_k x_p(t) + F_k x_r(t) + G_k r(t),\ t = t_k \\ u_r(t) &= C_r x_r(t) + D_r e(t) \end{aligned} \tag{4}$$

The main idea of this controller is to let free its after-reset state $x_r(t^+)$ (not necessarily equal to zero) and compute it and its parameters E_k, F_k, G_k, C_r and D_r in order to minimize a quadratic performance function of the form:

$$\begin{aligned} J_k = e^T(t_{k+1}) P_0 e(t_{k+1}) + \dot{e}^T(t_{k+1}) Q_0 \dot{e}(t_{k+1}) + \\ + \int_{t_k}^{t_{k+1}} e^T(s) P_1 e(s) ds, \end{aligned}$$

where P_0, Q_0 and P_1 are weighting vectors.

2.2 PI+CI controller

Following the classical condition of zero input, Baños and Vidal [2012, 2007] designed a PI+CI compensator to reduce considerably both the percentage of overshoot and settling time by resetting only a percentage of the integral term of a PI controller, namely P_{reset}. Its transfer function is given by

$$R(s) = k_p \left(1 + \frac{1 - P_{reset}}{\tau_i s} + \frac{P_{reset}\text{CI}}{\tau_i}\right), \tag{5}$$

where k_p is the proportional gain and τ_i is the integral time constant. It can be written in state space of the form of (1) with $\alpha_1 = 1, A_r = 0, B_r = \begin{bmatrix} 1 \\ 1 \end{bmatrix}, A_{R_r} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}, C_r = \begin{bmatrix} 0 & \frac{k_p}{\tau_i} \end{bmatrix}, D_r = k_p.$

2.3 FORE controller with feedforward

A feedforward controller was combined together with a traditional reset controller in Nesic et al. [2011] and Panni et al. [2012], as shown in Fig. 1. In order to avoid limit cycle, K should be chosen as the inverse of DC gain of the system, i.e.,

$$K = \begin{cases} -\dfrac{1}{C_p A_p^{-1} B_p}, & \text{if } A_p \text{ is invertible} \\ 0, & \text{otherwise} \end{cases} \tag{6}$$

In classic reset control, controller resets to zero when error is zero. Therefore, the feedforward controller adds $u = Kr = \frac{1}{P(0)} r$ to classic reset controller. As mentioned above, resetting to zero may cause limit cycle, but it can be eliminated by resetting to the non-zero value Kr. Actually, this feature is also common in reset control with fixed reset instants t_k and PC+CI controllers; all these three controllers will force the system to reset to Kr. More precisely, in reset control with fixed reset instants t_k, the controller parameters should be tuned to minimize x_r, which is not possible unless $\lim_{t \to \infty} u_r = Kr$. This condition was not proven in Zheng et al. [2007, 2008] but can be stated from provided experiment in the mentioned work. This condition is satisfied in PC+CI by a linear integrator and, in FORE with feedforward, by the feedforward gain K.

2.4 Fractional order proportional-CI

As another solution to eliminate limit cycle, a fractional order proportional CI –referred to as PCI$^\alpha$– was proposed in our previous work (HosseinNia et al. [2013b]), where a CI$^\alpha$ was used instead of the classic CI. The state space representation of PCI$^\alpha$ can be obtained by substituting $A_r = 0$, $B_r = 1$, $A_{R_r} = 0$, $C_r = \frac{k_p}{\tau_i}$ and $D_r = k_p$ in (1). Unlike integer order reset controllers, the asymmetrical transient response output waveform of CI$^\alpha$ makes the control signal to be different at the reset time, which may avoid the occurrence of limit cycle by adjusting its order adequately.

2.5 Fractional order PI+CI controller

So far we have seen, on the one hand, CI^α can increase the phase lag of the system and, on the other, PI+CI can be used to avoid limit cycles. Therefore, a fractional order PI+CI controller (both components of non-integer order, i.e., PI^α and CI^α) can be given by:

$$R(s) = k_p\left(1 + \frac{1-P_{reset}}{\tau_i s^\alpha} + \frac{P_{reset}\text{CI}^\alpha}{\tau_i}\right). \tag{7}$$

It can be written in state space of the form of (1) with $A_r = 0$, $B_r = \begin{bmatrix}1\\1\end{bmatrix}$, $A_{R_r} = \begin{bmatrix}1 & 0\\0 & 0\end{bmatrix}$, $C_r = \begin{bmatrix}0 & \frac{k_p}{\tau_i}\end{bmatrix}$, $D_r = k_p$. The describing function (DF) of PI^α+CI^α is expressed as

$$N(j\omega) = k_p\left(1 + \frac{1-P_{reset}}{\tau_i(j\omega)^\alpha} + \frac{P_{reset}}{\frac{4\tau_i}{\pi\omega^\alpha}\left(\sin\left(\alpha\frac{\pi}{2}\right) + \frac{\pi}{4}e^{-j\alpha\frac{\pi}{2}}\right)}\right). \tag{8}$$

Figure 2 shows the possibilities of the PI^α+CI^α compensator thanks to its two parameters, the reset ratio P_{reset} and the order α by using DF (8). In Fig. 2(a), the traditional PI+CI is compared with its base PI controller. It can be observed that it allows to achieve both higher phase margin and crossover gain frequency than the obtained with the base controller. Moreover, changing the order α in PI^α+CI^α, it is possible to obtain higher phase margin and crossover gain frequency than the PI+CI compensator when $P_{reset} = 0.5$ (see Fig. 2(b)). At the same time, the lower the value of α and P_{reset}, the higher both the phase margin and the crossover gain frequency. This means that a better performance in terms of speed of response and relative stability can be obtained by means of PI^α+CI^α compensator, overcoming limit cycle problem and improving the performance obtained with PI+CI.

3. GENERAL FORMS FOR RESET CONTROL

This section presents the main result of this paper: the introduction of a general SISO reset control, including fractional order dynamics, with both fixed and variable resetting to non-zero values.

3.1 Reset when error crosses zero

Taking into account the properties of the previous reset strategies, the following general fractional order reset controller –henceforth referred to as general reset controller– can be derived, where its state is reset to Kr when error crosses zero. It can be represented as

$$\begin{aligned} D^\alpha x_r(t) &= A_r x_r(t) + B_r e(t),\ e(t) \neq 0,\\ x_r(t^+) &= A_{R_r} x_r(t) + \frac{K}{n_{\mathscr{R}} c_r} B_{R_r} r,\ e(t) = 0,\\ u_r(t) &= C_r x_r(t) + D_r e(t), \end{aligned} \tag{9}$$

where matrix $A_{R_r} \in \mathbb{R}^{n_r \times n_r}$ identifies that subset of states $x_r(t)$ that are reset (the last $\mathscr{R}$ states) and has the form $A_{R_r} = \begin{bmatrix}I_{n_{\bar{\mathscr{R}}}} & 0\\0 & 0_{n_{\mathscr{R}}}\end{bmatrix}$, with $n_{\bar{\mathscr{R}}} = n_r - n_{\mathscr{R}}$ and $n_{\mathscr{R}}$ the length of the last $\mathscr{R}$ states, $B_{R_r} = \begin{bmatrix}0\\1\end{bmatrix}$, $C_r = c_r[0\ \ 1]$, $c_r \in \mathbb{R}$. And I and 0 denote identity and zero matrices with proper dimension, respectively.

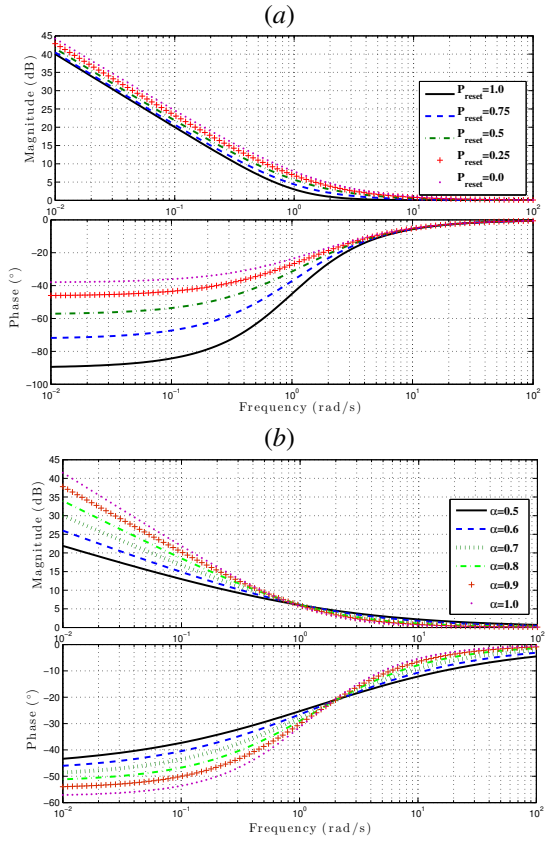

Fig. 2. Describing function (8) for different values of: (a) Reset percentage P_{reset} with $\alpha = 1$ (b) Order α with $P_{reset} = 0.5$. In both cases, $k_p = \tau_i = 1$

More specifically, controller (9) is a reset control with feedforward where its feedforward part becomes active when the first time error crosses zero. Actually, it activates the feedforward gain when it is necessary –the first reset time– in order to avoid limit cycles. Therefore, the general reset controller, unlike the reset controller with feedforward, maintains the same rise time as the base controller.

Let us denote the transfer function of the base controller as $R_{base}(s)$. According to Fig. 1, in presence of error, the closed-loop transfer function of the system controlled by the reset controller with feedforward and general reset controller are, respectively, $\frac{(K+R_{base}(s))P(s)}{1+R_{base}(s)P(s)}$ and $\frac{R_{base}(s)P(s)}{1+R_{base}(s)P(s)}$. Comparing these transfer functions with the transfer function of a classic controller (controller with no reset), it is obvious that only the general reset controller preserves some specification of the classic controller like rise time.

3.2 Reset periodically at fixed instants

Likewise, the controller described above can be reshaped to reset periodically when $t = t_k$, similarly to the reset control with fixed reset instants t_k, which will lead us to a more general reset controller as follows:

$$\begin{aligned} D^\alpha x_r(t) &= A_r x_r(t) + B_r e(t),\ t \neq t_k,\\ x_r(t^+) &= A_{R_r} x_r(t) + B_{R_r}\left(\frac{Kr - D_r e(t_k)}{n_{\mathscr{R}} c_r}\right),\ t = t_k,\\ u_r(t) &= C_r x_r(t) + D_r e(t). \end{aligned} \tag{10}$$

Due to the fact that reset happens periodically, and not necessarily when error is zero, it will take place at a variable non-zero value, which is function of both DC gain of the system and error.

4. EXAMPLES AND DISCUSSION

This section gives some examples of application of the aforementioned general and modified reset controllers for first and second order systems. It also provides some guidelines to be considered for designing reset controllers depending on the application. Fractional derivatives were simulated by Grünwald-Letnikov definition.

4.1 First order systems

In this first example, PI+CI, PCI$^\alpha$ and general reset strategies are going to be compared for the following first order system. Let us consider the system (Baños and Barreiro [2012])

$$\begin{array}{c} \dot{x}_p = -0.5x_p + 1.5u \\ y = x_p \end{array}, \tag{11}$$

whose transfer function is $P(s) = \frac{1.5}{s+0.5}$, controlled by a PI+CI of the form of (5) with $k_p = 2$, $\tau_i = 0.15$, and $P_{reset} = 0.21$ – the base PI controller was tuned to set the rising time to 0.31 s–. Now, consider controller (9) with a proportional-CI (PCI) resetting to $K = \frac{1}{P(0)}$: $A_r = 1, B_r = 0, C_r = \frac{k_p}{\tau_i}$ and $D_r = k_p$. With respect to PCI$^\alpha$, the parameters of the PI were chosen equal to the PI+CI case. In what concerns the selection of α, there is a trade off to overcome limit cycle and settling time: the lower its value, the higher the ability to avoid the limit cycle but the larger the settling time. For this reason, α was set to 0.9.

Simulation results are shown in Fig. 3 when applying the PI and PCI controller in (a) and using PI+CI, PCI$^\alpha$ and general reset control in (b). As observe in Fig. 3(a), PI and PCI cause an undesirable overshoot and limit cycle, respectively. In Fig. 3(b), it can be seen that the three controllers avoid the occurrence of limit cycle. Moreover, PI+CI and PCI$^\alpha$ controllers reduce the overshoot, whereas general reset control eliminate it completely. Taking into account the control signals, the system output when applying the PI tends to $K = 0.33$ when $t \to \infty$. By contrast, the PCI always resets to zero (when error is zero) which causes the limit cycle. This problem is solved in PI+CI by adding a linear integrator to the PCI, and in the PCI$^\alpha$ and the general reset controller by using a CI$^\alpha$ which will allow to reset to non-zero values. It can be observed that the control signal with the general reset controller reaches the value 0.33 after the first reset and, consequently, the overshoot is removed. For the PI+CI, the overshoot is reduced slightly. The PCI$^\alpha$ causes an undershoot in the system response, which is significantly lower than the overshoot obtained with the PI+CI and PI controllers.

Furthermore, Fig. 4 compares the behaviour of the system when applying PI$^\alpha$+CI$^\alpha$ for several values of α. It can be observed that the lower the value of α, the lower the overshoot and the faster the response. This is just to show the possibilities of extending PI+CI to fractional order.

4.2 Second order systems

This example firstly compares different strategies with error zero crossing and, then, controllers with periodic reset for second order systems.

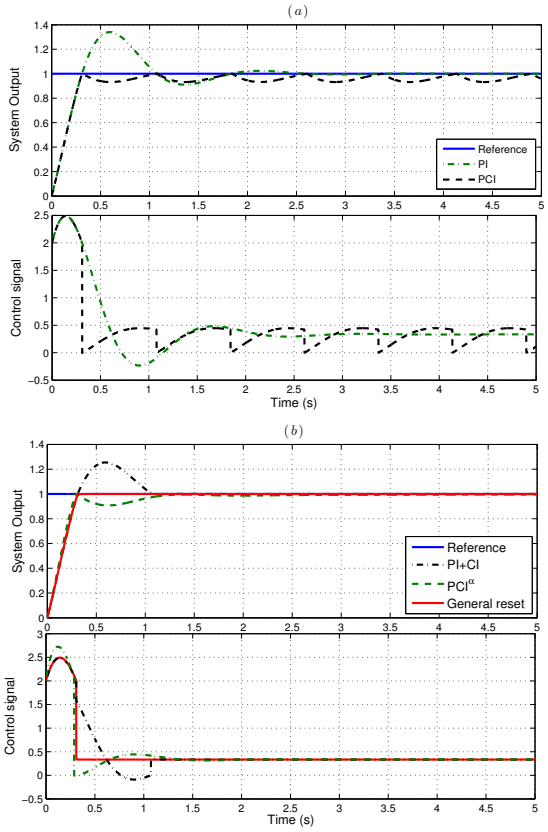

Fig. 3. Comparison of different reset controllers for first order system (11): (a) Using PI and PCI (b) Using PI+CI, PCI$^\alpha$ and general reset control

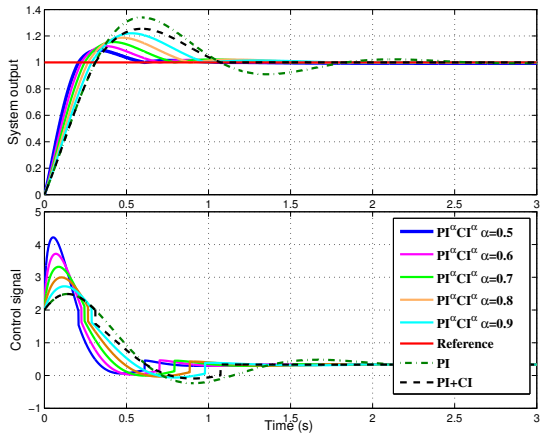

Fig. 4. Comparison of PI+CI and PI$^\alpha$+CI$^\alpha$ for different values of α for first order system (11)

Let us now consider the dynamics of a micro-actuator plant described by (Zheng et al. [2007, 2008]):

$$\begin{array}{c} \dot{x}_{p_1}(t) = x_{p_2}(t), \\ \dot{x}_{p_2}(t) = -a_1 x_{p_1}(t) - a_2 x_{p_2}(t) + bu(t), \\ y(t) = x_{p_1}(t) \end{array} \tag{12}$$

where x_{p_1} and x_{p_2} are position and velocity of the moving stage, with $a_1 = 10^6$, $a_2 = 1810$, and $b = 3 \times 10^6$. This system can be also given by its transfer function $P(s) = \frac{b}{s^2+a_2 s+a_1}$. Consider a reset controller with a PI as base linear controller and a periodic reset action, so:

$$\begin{aligned} \dot{x}_r(t) &= e(t),\ t \neq t_k \\ x_r(t^+) &= E_1 x_{p_1}(t) + E_2 x_{p_2}(t) + Gr(t),\ t = t_k, \\ u(t) &= \frac{k_p}{\tau_i} x_r(t) + k_p e(t) \end{aligned} \tag{13}$$

with $k_p = 0.08$ and $\tau_i = \frac{8}{3} \times 10^{-4}$. The optimization function J_k was minimized with the following parameters: $P_0 = 2.1, Q_0 = 10^{-6}$, and $P_1 = 0$. The reset time interval $\bigtriangledown t_k = t_k - t_{k-1}$ was fixed to 1 ms. Then, the optimal solution is given by the constant matrices $E_1 = -2.8 \times 10^{-4}$, $E_2 = -6.8 \times 10^{-7}$, and $G = 0.0014$. For the general controller, similar values were used with $\alpha = 1$.

Indeed, general reset controller, reset controller with feedforward and reset control with fixed reset instants t_k (13) reset to non-zero values. In particular, reset control with fixed reset instants t_k will reset to $\frac{k_p}{\tau_i}(E_1 x_{p_1} + E_2 x_{p_2} + Gr) + k_p e$. As time tends to infinity, the states x_{p_1} and x_{p_2} and error tend to r, 0 and 0, respectively. Therefore, the control signal u_r tends to $\frac{k_p}{\tau_i}(E_1 + G)r = 0.336$, which is very close to the feedforward gain for the unit step input, i.e., $K = \frac{1}{P(0)} = 0.333$. Likewise, reset control with fixed reset instants, resets when $t = t_k$ at each 1 ms, whereas general reset controller and reset controller with feedforward reset when $e = 0$.

The step responses and control signals when applying reset controller with feedforward and general reset controller are shown in Fig. 5. The performance of the system using a PI and a PCI were also obtained. As expected, reset controller with feedforward and general reset controller are able to eliminate the limit cycle caused by PCI, and this is because of the control signals reach the steady state value K. Figure 6 compares general reset control for different values of α. It can be seen that the higher the value of α, the lower the overshoot but the slower the response. Thus, a trade off between an integer and a fractional order general reset controller (in this case $\alpha = 1.1$) may be a good way to overcome both limit cycle and overshoot at the same time. The feedforward gain in the reset controller with feedforward and the fractional order CI in PCI$^\alpha$ cause different rise time in comparison with the classic PI controller.

Now, consider a general reset control with periodic resetting with the following parameters: $\alpha = 1$, $n_{\mathscr{R}} = 1$, $A_r = 0$, $B_r = 1$, $c_r = C_r = \frac{k_p}{\tau_i}$ and $D_r = k_p$. Simulation results using this controller and reset controller with reset instants are depicted in Fig. 7 for $t_k = 1$ ms. In comparison with the other strategies, it is seen that the overshoot is considerably reduced when applying controllers with periodic reset since they reset periodically before error reaches zero. However, it is worth mentioning that the general reset is capable of obtaining similar results than the controller proposed by Zheng et al. [2007, 2008] but without an optimization process, making the design of the reset controller simpler and more efficient. Notice that all the controllers have the same PI controller as base controller and, consequently, the system responses have similar rising time to the obtained with the classical PI controller, except with the PCI with feedforward controller.

For comparison purposes, Table 1 gives the integral of the squared error (ISE), the maximum value of the control signal, the overshoot and the rising time for system (12) when applying the designed controllers. As observed, the application of periodic reset, in comparison with traditional zero crossing reset, reduces considerably the ISE and the overshoot, but changes the rising time –it is increased. Considering controllers with fixed reset instants, the system response, in terms of ISE and overshoot, is slightly better when applying the reset control in Zheng et al. [2007, 2008]. However, as commented previously, the general reset control proposed in this work is easier to tune. On the other hand, among strategies with the classical reset condition, it is observed that the lowest value of the ISE is obtained when using the general reset controller. The worst result in terms of high control signal is obtained by the reset control with feedforward.

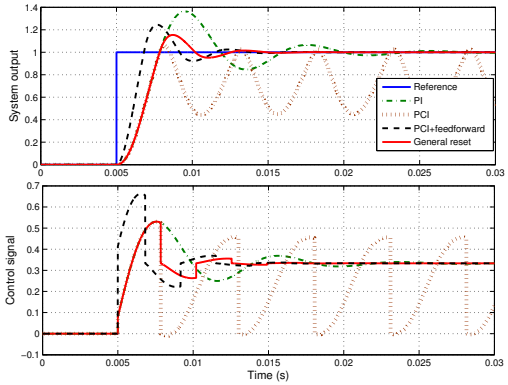

Fig. 5. Comparison of controllers with zero crossing reset for second order system (12)

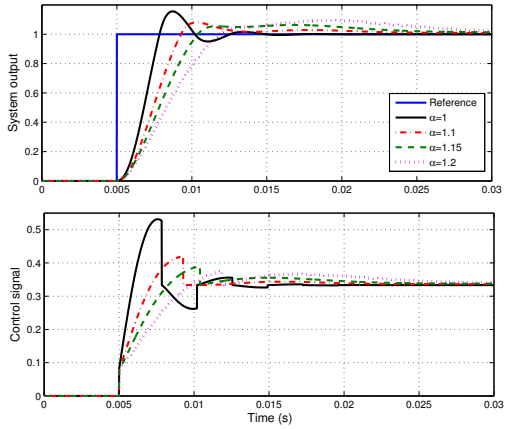

Fig. 6. Comparison of general reset control for different values of α for second order system (12)

4.3 Discussion

Taking into account the examples, the following remarks can be stated:

(1) Reset control with fixed reset instants t_k, PC+CI, PCI$^\alpha$, reset controller with feedforward and general reset controller are useful strategies to avoid the occurrence of limit cycle.
(2) A reset controller can avoid the occurrence of limit cycle when its control signal reaches a value equal to the inverse of the DC gain of the system multiplied by the input.
(3) General reset controller and reset controller with feedforward show the best performance for first order systems and are capable of eliminating the overshoot completely.
(4) In order to reduce the overshoot for higher order systems, it is recommended the use of general reset controller with

Table 1. Performance of the designed controllers for second order system (12)

	Strategies with zero crossing reset				Strategies with fixed reset instants	
	PCI	PI	PCI+Feedforward	General reset	Controller by Zheng et al. [2007, 2008]	General reset
ISE	650.3390	31.5634	4.8773	3.1660	0.0870	0.1595
Max(u)	0.5315	0.5305	0.6639	0.5325	0.7054	0.5646
M_p (%)	55.81	36.30	24.56	15.50	0.42	3.2
t_s (ms)	0.284	0.284	0.18	0.284	0.403	0.30

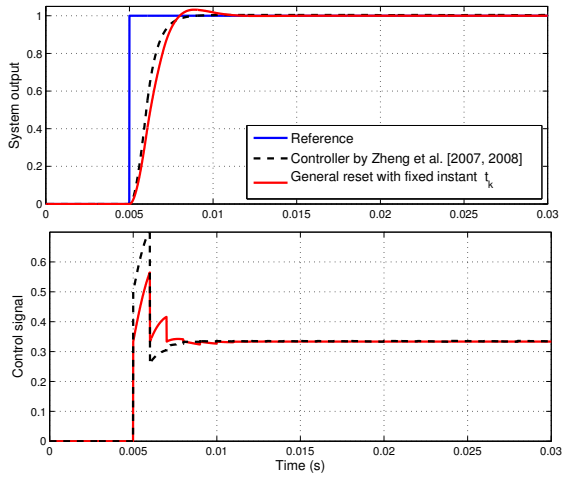

Fig. 7. Comparison of controllers with periodic reset for second order system (12)

periodic reset and reset control proposed by Zheng et al. [2007, 2008], due to their ability to switch when error is not necessarily zero. General reset control of fractional order can be another choice to reduce the overshoot in such systems.

(5) Despite the high ability of the reset control proposed by Zheng et al. [2007, 2008] in reducing the overshoot, its design is complicated due to the optimization process required. By contrast, the general reset controller (10) with periodic resets is simpler and, consequently, more useful.

(6) In general reset control, the feedforward part is active when the first reset happens. This feature makes this controller different from the one proposed by Nesic et al. [2011] and Panni et al. [2012], in which the feedforward controller is always on the loop. This fact causes that the rising time obtained by this reset controller is different from the obtained by the base one. On its behalf, the reset controller proposed by Zheng et al. [2007, 2008], due to its periodic reset, neither preserves the rise time of the base controller.

(7) For first order systems, in order to design a controller to have a response with no overshoot and a certain rise time, two steps are required: (i) tune the base controller to obtain the desired rise time, and (ii) apply general reset control.

5. CONCLUSIONS AND FUTURE WORK

This paper has investigated the main features of different modified reset control strategies, of integer and fractional order, to improve the performance of a system, especially in terms of prevention of limit cycle and traditional time domain specifications. A fractional order general reset control has been proposed by combining the more beneficial features of the previous controllers, which allows not only to avoid the occurrence of limit cycle but also to reduce, or even eliminate, the overshoot. A comparative study has been given to offer some guidelines to be considered when designing such controllers, depending on the application.

Since there is no a general agreement of the interpretation of state space representation of fractional systems, mainly concerning initial values (see e.g. Sabatier et al. [2013]), a further study should be carried out based on this issue in future work.

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