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Power optimal gate current profiles for the slew rate control of Smart Power ICs

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Abstract: Smart Power ICs are Power Switches with integrated control and protection functions. In order to meet the electromagnetic compatibility requirements, the output terminal slew rate has to be limited during the switching operation. In this context, special feedforward gate current profiles are widely used to control the switching slew rate. These profiles are typically determined on the basis of a linearized mathematical model of the Smart Power IC. However, due to the nonlinear characteristics of the IC, these profiles may lead to a reduced switching speed and thus to higher switching losses. In this work, an optimal control problem is considered which systematically accounts for the nonlinearities of the Power Switch, the switching losses and the limitation of the slew rate. In particular, a tailored mathematical model of the Smart Power IC is developed and parametrized. Based on this, the optimal control problem is formulated, numerically solved and the results are presented.

Keywords: Smart Power IC; gate current profile; gate driver; optimal control; slew rate control; feedforward design.

1. INTRODUCTION

In the last decades, Power Switches with integrated control and protection functions have become state of the art for the switching of middle and high current loads in automotive and industrial applications. These so-called Smart Power ICs (Murari et al., 2002) typically consist of a Power Switch, e.g., a Power MOSFET or an IGBT, a driver circuit to control the switching operation, and protection functions such as over temperature shutdown and load detection, see, e.g., Pribyl (1996). In state-of-the-art Smart Power ICs, the control and protection functions are typically implemented in the form of analog circuits. To increase the reusability of the circuit design and thus to reduce the development costs and time to market a digital realization seems to be promising and also allows to implement new features to meet future demands.
In order to meet the electromagnetic compatibility requirements and the customer demands, the current and voltage slew rate at the output terminal of the Power Switch has to be limited, see Oswald et al. (2011). The slew rate limitation results in a reduced switching speed and, consequently, in higher switching losses. In Smart Power ICs with a low on-resistance, the switching losses outweigh the total power dissipation and therefore have to be minimized. In order to minimize the switching losses, the slew rates not only have to be limited but they have to be actively controlled. To cope with this task, several, mostly analog, control strategies have been developed, see, e.g., Lefranc and Bergogne (2007); Wittig and Fuchs (2012) and Lobsiger and Kolar (2012). Because of the rather high hardware demands, digital closed-loop control strategies are not applicable and thus rather simple digital feedforward and adaptive feedforward strategies are employed in practice. In this context, so-called gate current profiles are used to control the switching operation. These profiles are applied to the Power Switch by a digital controllable gate current source. Gate current profiles are either used as a constant, (Schmitt et al., 2008), or iteratively adapted feedforward control, (Dang et al., 2011; Rose et al., 2010). Due to the highly nonlinear characteristics of the Smart Power IC, a gate current profile that controls the output terminal slew rates and simultaneously guarantees optimal switching speed cannot be obtained by a model inversion. Therefore, linearized models are often used to calculate such profiles. This typically results in limited slew rates but leads to a reduced switching speed and consequently to higher switching losses.
In this paper, gate current profiles which control the voltage or current slew rate at the output terminal of the Power Switch with respect to optimal switching speed and therefore power optimality are presented. The gate current profiles are obtained by solving an optimal control problem subject to the nonlinear mathematical model of the Smart Power IC and the maximum slew rate as path constraint. The presented method can be integrated in the hardware design process of the Smart Power ICs. Especially design questions regarding the necessary dynamics and current limits of the gate driver can be answered in a systematic way. Furthermore, the results can be used as an optimal initial guess for adaptive feedforward concepts. The work is structured as follows: a mathematical model of the Power Switch is presented in Section 2 and parametrized

in Section 3. The optimal control problem is formulated in Section 4 and numerical results are presented in Section 5.

2. MATHEMATICAL MODEL

The mathematical modeling is based on the simulation and circuit design of the Smart Power IC given in the Custom IC Design: Cadence Virtuoso Schematic environment. Because of the high complexity of the design and the partly unknown sub-circuit parameters an equivalent circuit is introduced, see Fig. 1. The equivalent circuit includes the n-Channel Power MOSFET T_1, the charge and discharge current sources, the charge pump and the ohmic-inductive load R_L and L_L. The charge pump increases the gate against the drain potential of the Power MOSFET and is modeled by the voltage source V_{cp} and the internal impedance R_{Vcp}. Furthermore, the current sources are each modeled by a current mirror, where $i_{g,10}$ and $i_{g,20}$ are the controllable reference currents and $i_{g,1}$ and $i_{g,2}$ are the output currents, respectively. The gate current $i_g = i_{g,1} - i_{g,2}$ serves as the control input for the switching operation. By applying a positive gate current $i_{g,1} > 0$ and $i_{g,2} = 0$, the input capacitances of the Power MOSFET are charged, the Power MOSFET is activated and the load is switched to the battery voltage V_{bat}. Similarly, by applying a negative gate current, $i_{g,2} > 0$ and $i_{g,1} = 0$, the input capacitances are discharged, the Power MOSFET is deactivated and the load is switched off.

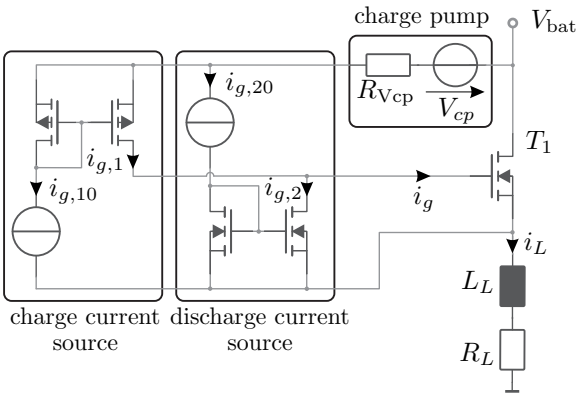

Fig. 1. Schematic of the Smart Power IC including the switching load in high-side configuration.

2.1 Power MOSFET

The turn-on and off characteristics of the Power MOSFET are determined by its parasitic capacitances and resistances and by the drain current which depends on the terminal voltage. In the large signal equivalent circuit shown in Fig. 2, the parasitic lead and substrate resistances are considered by means of the gate, drain and source resistors R_g, R_d and R_s which are assumed to be constant. The parasitic capacitances are summarized in the gate-source C_{gs}, drain-source C_{ds} and gate-drain C_{gd} capacity. Since the depletion layer contributes to the parasitic capacitances, they vary with the terminal voltage and are defined as $C = \mathrm{d}Q/\mathrm{d}v$ with the charge Q and the terminal voltage v. More precisely, C_{gs} is the combination of the oxide and the depletion layer capacitance of the

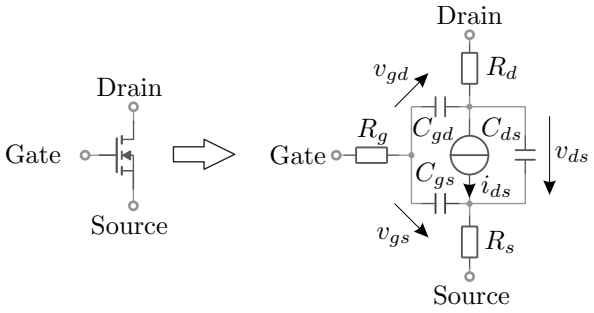

Fig. 2. Schematic and large signal equivalent circuit of the n-Channel Power MOSFET.

SI-SO2 interface and is assumed to be independent of the terminal voltage, i.e. $C_{gs} = \text{const.}$, see Mohan et al. (2003). Moreover, C_{ds} results from the $p^+n^-n^+$-diode between the drain and source terminal, see Schröder (2006), and is approximated with the capacitance of a pn-junction in the form

$$C_{ds}(v_{ds}) = \frac{C_{ds,0}}{\left(1 - \frac{v_{ds}}{\phi_{c,ds}}\right)^{n_{c,ds}}}, \tag{1}$$

where $C_{ds,0}$ denotes the drain-source capacitance at zero drain-source voltage $v_{ds} = 0$, $\phi_{c,ds}$ is the barrier potential and $n_{c,ds}$ is the grading coefficient, cf. Allen and Holberg (2002). Finally, C_{gd} is determined by the oxide capacitance and the drain depletion layer beneath the gate oxide, see, e.g., Baliga (2008). The latter exists only if the drain potential is more positive than that of the gate. When the gate is more positive, C_{gd} is dominated by the gate oxide capacitance $C_{gd} = C_{gd,0} = \text{const.}$ for $v_{gd} \geq 0$, see Grant and Gowar (1989). Otherwise the depletion layer enlarges with v_{gd} and C_{gd} is approximately given by

$$C_{gd}(v_{gd}) = \frac{C_{gd,0}}{\left(1 - \frac{v_{gd}}{b_{c,gd}}\right)^{a_{c,gd}}} \quad \text{for} \quad v_{gd} < 0, \tag{2}$$

with the constant parameters $b_{c,gd}$ and $a_{c,gd}$. In order to achieve continuous differentiability, $C_{gd}(v_{gd})$ is approximated by a polynomial of third order in a $\delta_{v_{gd}}$-neighborhood of $v_{gd} = 0$ resulting in

$$C_{gd}(v_{gd}) = \begin{cases} C_{gd,0}, & v_{gd} > \delta_{v_{gd}} \\ C_{gd,0} \sum_{i=0}^{3} a_i (-v_{gd})^i, & \delta_{v_{gd}} \geq v_{gd} \geq -\delta_{v_{gd}} \\ \frac{C_{gd,0}}{\left(1 - \frac{v_{gd}}{b_{c,gd}}\right)^{a_{c,gd}}}, & v_{gd} < -\delta_{v_{gd}} \end{cases} \tag{3}$$

where $a_i, i = 0,1,2,3$ constitute constant parameters. The voltage dependency of the drain current is considered by the drain current source $i_{ds} = i_{ds}(v_{gs}, v_{ds})$ which is modeled using the core of the so-called EKV (Enz-Krummenacher-Vittoz) model, see, e.g., Enz and Vittoz (2006); Chauhan et al. (2006). It describes the drain current in the form of a single, continuous and continuously differentiable function

$$i_{ds} = I_s \left(i_F - i_R\right), \tag{4a}$$

with the specific current I_s, the normalized forward

$$i_F = \left[\ln\left(1 + \exp\left(\frac{v_p}{2V_t}\right)\right)\right]^2 (1 + \lambda v_{ds}) \tag{4b}$$

and reverse current

$$i_R = \left[\ln\left(1+\exp\left(\frac{v_p - v_{ds}}{2V_t}\right)\right)\right]^2, \tag{4c}$$

where V_t denotes the thermal voltage, λ the channel length modulation factor and

$$v_p = \frac{v_{gs} - V_{th}}{n} \tag{4d}$$

the pinch-off voltage with the threshold voltage V_{th} and the slope factor n. The slope factor is assumed to be constant and the forward current i_F is phenomenologically extended with the approximation of the channel length modulation $1 + \lambda v_{ds}$.

2.2 Discharge Current Source

The discharge current source is modeled by a current mirror consisting of the transistors T_{21} and T_{22} with the reference current $i_{g,20}$, the output current $i_{g,2}$ and the output terminal voltage $v_{ds,22}$, cf., Fig. 3. The terminal

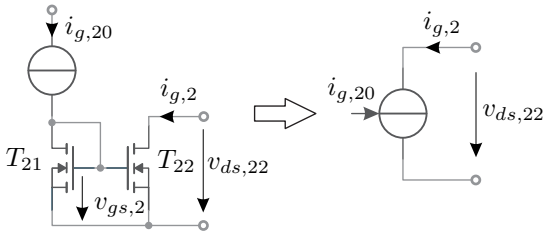

Fig. 3. Large signal equivalent circuit of the discharge current source.

voltage $v_{ds,22}$ strongly varies during a switching operation due to its dependency on v_{gs}. Therefore, T_{22} operates in all regions and thus the all-region approach (4) is used to model the output current as

$$\begin{aligned} i_{g,2} =& I_{s,22}\left(\left[\ln\left(1+\exp\left(\frac{v_{p,22}}{2V_{t,2}}\right)\right)\right]^2 (1+\lambda_{22} v_{ds,22})\right. \\ &\left. - \left[\ln\left(1+\exp\left(\frac{v_{p,22}-v_{ds,22}}{2V_{t,2}}\right)\right)\right]^2\right). \end{aligned} \tag{5a}$$

Here, $I_{s,22}$ denotes the specific current, $V_{t,2}$ the thermal voltage, λ_{22} the channel length modulation factor and

$$v_{p,22} = v_{gs,2} - V_{th,22} \tag{5b}$$

the pinch-off voltage with the threshold voltage $V_{th,22}$ and the common gate-source voltage $v_{gs,2}$. Here, the slope factor was set to 1. Furthermore, $v_{gs,2}$ is determined by solving the drain current equation of T_{21}. Due to the common gate-drain potential of T_{21} and $v_{gs,2} > V_{th,21}$, T_{21} operates only in the saturation mode. Using the first order MOSFET model, see Arora (2007), the common gate-source voltage in saturation mode reads as

$$v_{gs,2} = \sqrt{\frac{2 i_{g,20}}{K_{21}}} + V_{th,21}, \tag{6}$$

with the gain factor K_{21} and the threshold voltage $V_{th,21}$. To obtain an exact model of the current source dynamics, the parasitic resistances as well as the capacitances of T_{21} and T_{22} have to be modeled too. However, because of the relatively small terminal currents, the parasitic resistances are negligible. Furthermore, the parasitic capacitances are rather small compared to those of T_1, thus, the dynamics of the current source are considerably faster compared to the Power MOSFET. In order to obtain a compact mathematical model and by considering at the same time the current source dynamics, a first order lag element

$$T_{f,2}\frac{\mathrm{d}v_{ds,22f}}{\mathrm{d}t} + v_{ds,22f} = v_{ds,22} \tag{7}$$

is used, where $T_{f,2}$ denotes the time constant and $v_{ds,22f}$ is the delayed terminal voltage. Replacing $v_{ds,22}$ by $v_{ds,22f}$ in (5) yields, together with (6), the input/output behavior of the discharge current source $i_{g,2} = i_{g,2}\left(i_{g,20}, v_{ds,22f}\right)$. The presented modeling approach is also directly applicable to the charge current source but will be omitted here for the sake of brevity.

2.3 Large-Signal Model

Complementing the equivalent circuit of Fig. 1 with the large signal equivalent circuits from Fig. 2 and Fig. 3 yields the large signal model of the Smart Power IC depicted in Fig. 4. Additionally, the offset currents $i_{\mathrm{off},1}$

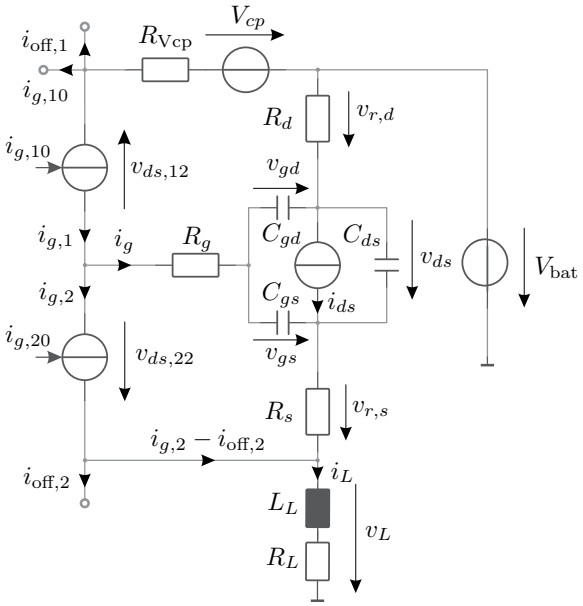

Fig. 4. Large signal model of the Smart Power IC.

and $i_{\mathrm{off},2}$ accounting for miscellaneous measurement and control circuits are added and are assumed to be constant. By applying Kirchhoff's circuit laws together with the constitutive equations and the approximations $v_{r,d} \approx i_L R_d$ and $v_{r,s} \approx i_L R_s$ and by neglecting the gate resistance ($R_g = 0$), the mathematical model of the Smart Power IC takes the form

$$\frac{\mathrm{d}}{\mathrm{d}t} i_L = \frac{1}{L_L}\Big(V_{\mathrm{bat}} + v_{gd} - v_{gs} - i_L\left(R_s + R_L + R_d\right)\Big) \tag{8a}$$

$$\begin{aligned} \frac{\mathrm{d}}{\mathrm{d}t} v_{gd} =& \frac{C_{ds}\left(v_{ds}\right)}{C(v_{gs}, v_{gd})}\Big(i_{g,1}\left(i_{g,10}, v_{ds,12f}\right) \\ &- i_{g,2}\left(i_{g,20}, v_{ds,22f}\right)\Big) \\ &+ \frac{C_{gs}}{C(v_{gs}, v_{gd})}\Big(-i_L + i_{ds}\left(v_{gd}, v_{gs}\right) - i_{\mathrm{off},2} \\ &+ i_{g,1}\left(i_{g,10}, v_{ds,12f}\right)\Big) \end{aligned} \tag{8b}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}v_{gs} = \frac{C_{ds}\left(v_{ds}\right)}{C(v_{gs},v_{gd})}\Big(i_{g,1}\left(i_{g,10},v_{ds,12f}\right) - i_{g,2}\left(i_{g,20},v_{ds,22f}\right)\Big) + \frac{C_{gd}\left(v_{gd}\right)}{C(v_{gs},v_{gd})}\Big(i_L - i_{ds}\left(v_{gd},v_{gs}\right) + i_{\mathrm{off},2} - i_{g,2}\left(i_{g,20},v_{ds,22f}\right)\Big) \tag{8c}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}v_{ds,12f} = \frac{1}{T_{f,1}}\Big(v_{gd} - V_{cp} - R_d i_L - v_{ds,12f} + \big(i_{\mathrm{off},1} + i_{g,1}\left(i_{g,10},v_{ds,12f}\right) + i_{g,10}\big)R_{\mathrm{Vcp}}\Big) \tag{8d}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}v_{ds,22f} = \frac{1}{T_{f,2}}\Big(v_{gs} + R_s i_L - v_{ds,22f}\Big) \tag{8e}$$

with the equivalent capacitance

$$C(v_{gs},v_{gd}) = \Big(C_{gd}\left(v_{gd}\right) + C_{gs}\Big)C_{ds}\left(v_{ds}\right) + C_{gd}\left(v_{gd}\right)C_{gs}. \tag{8f}$$

Here, $C_{ds}\left(v_{ds}\right)$ and $C_{gd}\left(v_{gd}\right)$ are according to (1) and (3), and $v_{ds} = v_{gs} - v_{gd}$. The drain current $i_{ds}\left(v_{gd},v_{gs}\right)$ follows from (4) and the output currents $i_{g,1}\left(i_{g,10},v_{ds,12f}\right)$ and $i_{g,2}\left(i_{g,20},v_{ds,22f}\right)$ are due to (5) and (6).

3. PARAMETER IDENTIFICATION

The parameter identification is based on the circuit elements and the simulation results of the full circuit design given in the CADENCE CUSTOM IC DESIGN environment and the data sheet of the Power MOSFET: BSC020N03LS.

(1) The drain current source parameters V_t, I_s, V_{th}, n and λ are identified by means of a nonlinear least squares fitting of the transfer and output characteristics of the Power MOSFET given in the full circuit design.
(2) The parameters of the charge K_{11}, $V_{th,11}$, $V_{th,12}$, $V_{t,1}$, $I_{s,12}$, λ_{12} and the discharge current source K_{21}, $V_{th,21}$, $V_{th,22}$, $V_{t,2}$, $I_{s,22}$ and λ_{22} are identified by a nonlinear least squares fitting of the input/output characteristics of the full circuit current sources. The time constants of the first order lag elements $T_{f,1}$ and $T_{f,2}$ are parametrized by means of simulation results.
(3) The identification of the capacitance parameters $C_{gd,0}$, $C_{gs,0}$, $C_{ds,0}$, $\phi_{c,ds}$, $n_{c,ds}$, $b_{c,gd}$ and $a_{c,gd}$ is based on the characteristics of the input, output and reverse capacitance C_{rss}, C_{iss} and C_{oss} from the data sheet.
(4) The parasitic resistances R_d and R_s, the offset currents $i_{\mathrm{off},1}$ and $i_{\mathrm{off},2}$, the model parameters of the charge pump V_{cp} and R_{Vcp} as well as the battery voltage V_{bat} are extracted from the full circuit design.

The identification results are summarized in Table 1.

4. OPTIMAL CONTROL PROBLEM

The mathematical model (8) can be written in the form

$$\frac{\mathrm{d}}{\mathrm{d}t}\mathbf{x} = \mathbf{f}(\mathbf{x},\mathbf{u}), \qquad \mathbf{x}(0) = \mathbf{x}_0, \tag{9}$$

with the state vector $\mathbf{x}^{\mathrm{T}} = [i_L\ v_{gd}\ v_{gs}\ v_{ds,12f}\ v_{ds,22f}]$, the initial condition $\mathbf{x}_0 \in \mathbb{R}^5$ and the control input $\mathbf{u}^{\mathrm{T}} = [i_{g,10}\ i_{g,20}]$. The control objective is to find an optimal control input $\mathbf{u}^* \in \mathcal{U} = [\mathbf{u}^-, \mathbf{u}^+]$ that minimizes the switching losses $\int i_L v_{ds}\,\mathrm{d}t = \int x_1(x_3 - x_2)\,\mathrm{d}t$ and takes into account the current slew rate $\mathrm{d}i_L/\mathrm{d}t$ or the voltage slew rate $\mathrm{d}v_{ds}/\mathrm{d}t$ at the output terminal of the Power Switch. For this, the optimal control problem

$$\begin{aligned} \min_{\mathbf{u}\in\mathcal{U}} \quad & J(\mathbf{x}) = \int_{t_0^j}^{t_f^j} x_1(x_3 - x_2)\,\mathrm{d}t \\ \text{s.t.} \quad & \frac{\mathrm{d}}{\mathrm{d}t}\mathbf{x} = \mathbf{f}(\mathbf{x},\mathbf{u}), \quad \mathbf{x}(t_0^j) = \mathbf{x}_0^j \\ & \mathbf{u} = \begin{bmatrix} i_{g,10} \\ i_{g,20} \end{bmatrix} \in \mathcal{U} = \begin{bmatrix} i_{g,10}^- & i_{g,10}^+ \\ i_{g,20}^- & i_{g,20}^+ \end{bmatrix} \\ & s^u \le s\left(\mathbf{x},\mathbf{u}\right) \le s^l \end{aligned} \tag{10}$$

is formulated. By means of the Lagrange density $x_1(x_3 - x_2)$ of the cost function $J(\mathbf{x})$ the minimization of the occurring power losses during the switching operation $t \in [t_0^j, t_f^j]$, $j \in \{\mathrm{on}, \mathrm{off}\}$ is assured. Furthermore, $\mathbf{x}_0^j$ represents the initial state for the on and off switching operation, respectively. The input $\mathbf{u}$ is constrained with the upper and lower physical limits of the charge and discharge reference current, $i_{g,10}^-$, $i_{g,10}^+$ and $i_{g,20}^-$, $i_{g,20}^+$, respectively. To guarantee the switching of the Power MOSFET, $i_{g,10}^-$ and $i_{g,20}^-$ are assumed to be positive. The term $s^l \le s(\mathbf{x},\mathbf{u}) \le s^u$ refers to the path constraint in order to limit the current or voltage slew rate s to its desired upper and lower limit s^u and s^l. Note that for the switch-on operation only the charge current source and for the switch-off operation only the discharge current source is used, i.e. $\mathbf{u}^{\mathrm{T}} = [i_{g,10}\ 0]$ and $\mathbf{u}^{\mathrm{T}} = [0\ i_{g,20}]$. Summarizing, four different cases of the optimal control problem have to be solved:

(1) The current slew rate $\mathrm{d}i_L/\mathrm{d}t$ during the switch-on operation $j = \mathrm{on}$ is controlled by $\mathbf{u}^{\mathrm{T}} = [i_{g,10}\ 0]$. The path constraint is set to $s = \mathrm{d}i_L/\mathrm{d}t$ and the desired upper and lower limits are $s^u = \dot{i}_{L,d}$ and $s^l = -\dot{i}_{L,d}$.

(2) The current slew rate $\mathrm{d}i_L/\mathrm{d}t$ during the switch-off operation $j = \mathrm{off}$ is controlled by $\mathbf{u}^{\mathrm{T}} = [0\ i_{g,20}]$. The path constraint is set to $s = \mathrm{d}i_L/\mathrm{d}t$ and the desired

Table 1. Model parameters.

Symbol	Value	Unit	Symbol	Value	Unit
R_s	50	$\mu\Omega$	K_{11}	11	$\mu\mathrm{A/V}^2$
R_d	336	$\mu\Omega$	$V_{th,11}$	2.17	V
n	5.97	1	$V_{th,12}$	2.15	V
λ	1.088	V	λ_{12}	2957	V
V_{th}	2.48	V	$T_{f,1}$	4	μs
I_s	3.34	A	$I_{s,12}$	0.135	μA
V_t	25	mV	$V_{t,1}$	25	mV
$C_{gd,0}$	1284	pF	K_{21}	248	$\mu\mathrm{A/V}^2$
$C_{gs,0}$	5321	pF	$V_{th,21}$	2.12	V
$C_{ds,0}$	5148	pF	$V_{th,22}$	2.11	V
$\phi_{c,ds}$	7.25	V	λ_{22}	30	V
$n_{c,ds}$	0.9	1	$T_{f,2}$	1.5	μs
$b_{c,gd}$	0.38	V	$I_{s,22}$	2.796	μA
$a_{c,gd}$	0.5	1	$V_{t,2}$	25	mV
$\delta_{v_{gd}}$	0.2	V	V_{cp}	6	V
a_0	0.94	1	R_{Vcp}	30	kΩ
a_1	-0.54	1/V	$i_{\mathrm{off},1}$	57.7	μA
a_2	-0.87	$1/\mathrm{V}^2$	$i_{\mathrm{off},2}$	57.7	μA
a_3	1.59	$1/\mathrm{V}^3$	V_{bat}	13	V

upper and lower limits are $s^u = \dot{i}_{L,d}$ and $s^l = -\dot{i}_{L,d}$.

(3) The voltage slew rate $\mathrm{d}v_{ds}/\mathrm{d}t$ during the switch-on operation $j = \text{on}$ is controlled by $\mathbf{u}^{\mathrm{T}} = [i_{g,10}\ 0]$. The path constraint is set to $s = \mathrm{d}v_{ds}/\mathrm{d}t$ and the desired upper and lower limits are $s^u = \dot{v}_{ds,d}$ and $s^l = -\dot{v}_{ds,d}$.

(4) The voltage slew rate $\mathrm{d}v_{ds}/\mathrm{d}t$ during the switch-off operation $j = \text{off}$ is controlled by $\mathbf{u}^{\mathrm{T}} = [0\ i_{g,20}]$. The path constraint is set to $s = \mathrm{d}v_{ds}/\mathrm{d}t$ and the desired upper and lower limits are $s^u = \dot{v}_{ds,d}$ and $s^l = -\dot{v}_{ds,d}$.

5. NUMERICAL RESULTS OF THE OPTIMAL CONTROL PROBLEM

The optimal control problem (10) is formulated as a finite-dimensional optimization problem by means of full discretization using the trapezoidal rule and assuming a constant control input in the respective time interval, see, e.g., Betts (2001). The finite-dimensional optimization problem is solved using MATLAB in combination with the Sequential Quadratic Programming method from the Large-Scale Nonlinear Programming package SNOPT, see Gill et al. (2006). The optimization was carried out for the time intervals $t^{\text{on}} \in [10, 46]\,\mu\text{s}$ and $t^{\text{off}} \in [30, 66]\,\mu\text{s}$ with 240 discretization points for each interval. Afterwards, a simulation was performed in MATLAB, where the maximum value of the optimal control input was assigned outside the time intervals t^{on} and t^{off}. The numerical results for different voltage and current slew rates are summarized in Fig. 5(a) and Fig. 5(b). In detail, the first row presents the gate current profiles $i_{g,10}$ and $i_{g,20}$ for the switch-on and switch-off operation. In the second and third row, the resulting output terminal voltage v_{ds} and the respective slew rate $\mathrm{d}v_{ds}/\mathrm{d}t$ are depicted and in the fourth and fifth row, the load current i_L and the respective slew rate $\mathrm{d}i_L/\mathrm{d}t$ are shown. Finally, the sixth row presents the switching losses $\int i_L v_{ds}\,\mathrm{d}t$.
The results show that by means of the calculated gate current profiles, $\mathrm{d}v_{ds}/\mathrm{d}t$ and $\mathrm{d}i_L/\mathrm{d}t$ is not only limited, but controlled to their desired maximum slew rate. As long as no slew rate constraint is violated, the gate current profile is at its maximum value. Thus, maximal switching speed and therefore minimal switching losses are achieved. This arises directly from the consideration of the switching losses in the cost function (10). A constant gate current profile with a lower maximum value would only change the peak of the slew rate. Clearly, this would result in higher switching losses.
A closer look at the gate current profiles shows that the profiles for the switch-on and switch-off operation are not identical. This is due to the different physical characteristics of the charge and discharge current sources.
Because of the inductive switching, the current lags behind the voltage. Therefore, by controlling the current slew rate, the voltage slew rate exhibits small spikes shortly before the current slew rate is active. This must be considered for voltage related electromagnetic compatibility problems.

6. CONCLUSION AND FUTURE WORK

In this work, optimal gate current profiles are derived which simultaneously control the current or voltage slew rate at the output terminal of a Smart Power IC and minimize the switching losses. For this, a tailored mathematical model of the Smart Power IC was developed and identified. Based on this model, an optimal control problem that limits the current or voltage slew rate to a predefined value during the switch-on and off operation was formulated and numerically solved.
The presented method can be directly integrated in the hardware design process of the Smart Power ICs. In particular, design questions regarding the necessary dynamics and current limits of the charge and discharge current source can be answered in a systematic way. Due to model uncertainties and temperature dependencies the direct application of the gate current profiles in pure feedforward control strategies is of limited practical use. However, the profiles can be utilized as an optimal initial guess for adaptive feedforward strategies. Such a strategy is presented in Blank et al. (2014) using an iterative learning control strategy that adapts the gate current profile in real time.

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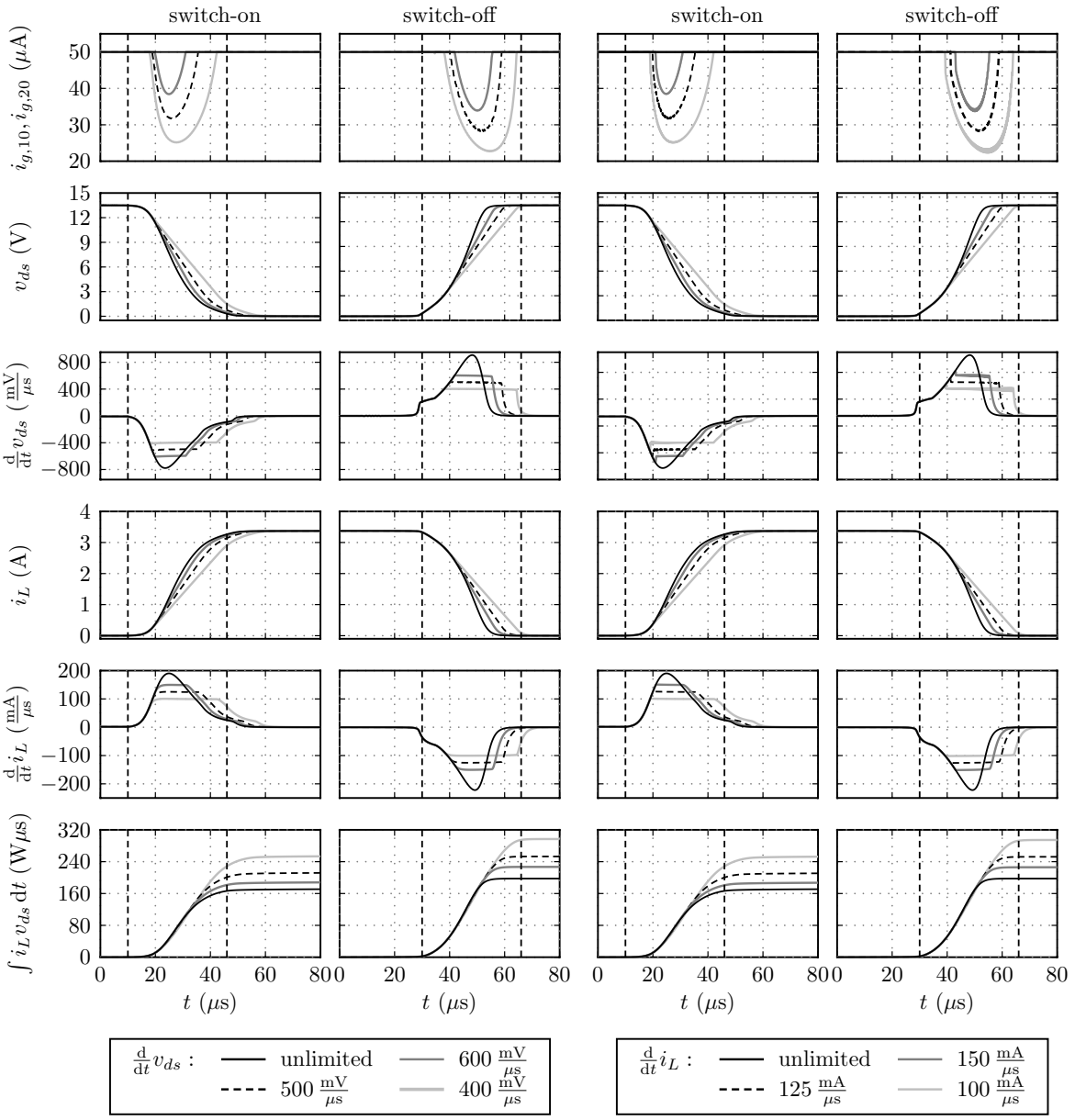

(a) Control results of the voltage slew rate. (b) Control results of the current slew rate.

Fig. 5. Numerical results of the optimal control problem for the switch-on and switch-off operation.

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