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Predictive Ratio Control of Multizone Thermal Processing System in Lithography

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Abstract: Baking of semiconductor substrate is common and critical to photoresist processing in the lithography sequence. Temperature uniformity control is an important issue in photoresist processing with stringent specifications and has a significant impact on the linewidth or critical dimension (CD). In this work, we present the development of a ratio control strategy for controlling temperature uniformity of a silicon wafer substrate. Traditional approach in ratio control does not consider interaction among the different input, our approach takes into consideration the interaction between the different heating zone of the novel multizone thermal system developed by us. The resultant model-based GPC PID controller is designed and tested on the multizone thermal system. Simulation results shows that spatial temperature uniformity can be controlled to within 1^oC and 0.1^oC during transient and steady-state operating condition respectively.

1. INTRODUCTION

Ratio control, a special type of feedforward control, has been widely used in the process industries, in applications such as chemical dosing, water treatment, chlorination, mixing vessels and waste incinerators (Seborg, et al. [1989]). The objective of the ratio control is to maintain the ratio of two variables at a specified value α. The actual ratio of the two process variables is controlled rather than controlling the individual variables. Ratio control is usually used in system with coupling, for example, in the blending operations it is desired to keep the ratio between different flows constant. Ratio control is commonly implemented using simple series and parallel Ratio stations (Seborg, et al. [1989] Shinskey [1981] and Shinskey [1996]).

While ratio control of decoupled processes is well established, the problem and challenges become significantly more complex for interacting processes. The process interactions set the stage for a full multivariable control problem where ratio control is to be achieved for the process variables. There are two control objectives considered in the paper. First, the ratio between the outputs $y_1(t)$ and $y_2(t)$ is to be kept to be within a tight threshold around α. Secondly, with this ratio thus maintained, the process variables are required to track changing setpoint profiles. The approach adopted in the paper is a model-based one. First, a model for the interacting processes is obtained. A two-inputs two-outputs interactive process model is considered in this paper. Based on this model, predictive controllers are realised using Generalized Predictive Control (GPC) design methodology to maintain tight control in the presence of interactions. General Predictive Control (GPC) method, proposed in (Clarke, et al. [1987]), has become one of the most popular Model Predictive Control methods used in the industries. GPC has the features that the performance index includes the prediction horizon and control horizon and the weighting factor. The control signals are derived by minimizing the cost function on the future control inputs and re-calculated receding from their horizons at each sampling time. However, although GPC can give good performance, GPC is still not used in many industrial processes because of the hardware, commissioning and maintenance costs. Acknowledging this resistance to the use of GPC, the GPC control adopted in this paper will be moulded to function from within a PID structure. The results extend present ones in GPC-based PID controller design for SISO systems (Tan, et al. [2002] and Tan, et al. [2000]) to multivariable systems. In (Moradi [2003]), predictive PID controller for MIMO systems was proposed.

In this paper, the proposed predictive ratio control is applied to the wafer temperature uniformity control in the lithography. Temperature uniformity control is an important issue in photoresist processing with stringent specifications and has significant impact on the linewidth or critical dimension (CD). The proposed method is an *in situ* approach to real-time control the wafer temperature uniformity during the baking process in microlithography. The GPC-based PID controller design is in the state space representation. Section 2 presents the derivation of the proposed method for the interacting process. In Section 3, the background of the wafer temperature uniformity control to which the proposed method is applied is introduced. In Section 4, the simulation results are furnished to illustrate the effectiveness of the proposed method.

2. PREDICTIVE CONTROL DESIGN

In this paper, a two inputs and two outputs system is studied. The transfer functions that relate all inputs and

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outputs are in the forms of first order. The investigated process is given by

$$
\begin{aligned}
Y_1(s) &= \frac{k_{11}}{T_{11}s+1}U_1(s) + \frac{k_{12}}{T_{12}s+1}U_2(s),\\
Y_2(s) &= \frac{k_{21}}{T_{21}s+1}U_1(s) + \frac{k_{22}}{T_{22}s+1}U_2(s),
\end{aligned}
\tag{1}
$$

Then, it can be written as the discrete time form,

$$
\begin{aligned}
y_1(z) &= \frac{b_{11}}{z+a_{11}}u_1(z) + \frac{b_{12}}{z+a_{12}}u_2(z),\\
y_2(z) &= \frac{b_{21}}{z+a_{21}}u_1(z) + \frac{b_{22}}{z+a_{22}}u_2(z).
\end{aligned}
\tag{2}
$$

Let $e_1 = r_1 - y1$ and $e_2 = r_2 - y2$, where r_1 and r_2 are the setpoints for the bakeplate temperatures of zone 1 and zone 2. Here ratio control is applied to keep the ratio between two process variables y_1 and y_2 at the desired ratio α. Equation (2) can be rearranged in the difference equation regarding to the error,

$$
\begin{aligned}
&e_1(k+2) + (a_{11}+a_{12})e_1(k+1) + (a_{11}a_{12})e_1(k) =\\
&-b_{11}(u_1(k+1) + a_{12}u_1(k)) - b_{12}(u_2(k+1) + a_{11}u_2(k))\\
&+r_1(k+2) + (a_{11}+a_{12})r_1(k+1) + (a_{11}a_{12})r_1(k)\\
&e_2(k+2) + (a_{21}+a_{22})e_2(k+1) + (a_{21}a_{22})e_2(k) =\\
&-b_{21}(u_1(k+1) + a_{22}u_1(k)) - b_{22}(u_2(k+1) + a_{21}u_2(k))\\
&+r_2(k+2) + (a_{21}+a_{22})r_2(k+1) + (a_{21}a_{22})r_2(k).
\end{aligned}
\tag{3}
$$

Introduce variables $U(k)$ and $\tilde{r}(k)$ defined by $U(k) = [u_1(k) \quad u_2(k)]^T$ and $\tilde{r}(k) = [\tilde{r}_1(k) \quad \tilde{r}_2(k)]^T$, where $\tilde{r}_1(k) = r_1(k+2) + (a_{11}+a_{12})r_1(k+1) + (a_{11}a_{12})r_1(k)$ and $\tilde{r}_2(k) = r_2(k+2) + (a_{21}+a_{22})r_2(k+1) + (a_{21}a_{22})r_2(k)$.

To formulate the state space description in the observer canonical form, define the state vector,

$$
X(k) = \begin{bmatrix} x_1(k) \\ x_{1d}(k) \\ \theta_1(k) \\ x_2(k) \\ x_{2d}(k) \\ \theta_2(k) \end{bmatrix},
\tag{4}
$$

where $\theta_1(k) = \sum_{i=0}^{k-1} e_1(i)$ and $\theta_2(k) = \sum_{i=0}^{k-1} e_2(i)$. Let $x_1(k) = e_1(k)$ and $x_2(k) = e_2(k)$. Therefore, Equation (3) can be written in observer canonical state-space form as

$$
\begin{aligned}
X(k+1) = &\begin{bmatrix}
-(a_{11}+a_{12}) & 1 & 0 & 0 & 0 & 0\\
-(a_{11}a_{12}) & 0 & 0 & 0 & 0 & 0\\
1 & 0 & 1 & 0 & 0 & 0\\
0 & 0 & 0 & -(a_{21}+a_{22}) & 0 & 0\\
0 & 0 & 0 & -(a_{21}a_{22}) & 0 & 0\\
0 & 0 & 0 & 1 & 0 & 1
\end{bmatrix} X(k)\\
&+ \begin{bmatrix}
-b_{11} & -b_{12}\\
-b_{11}a_{12} & -b_{12}a_{11}\\
0 & 0\\
-b_{21} & -b_{22}\\
-b_{21}a_{22} & -b_{22}a_{21}\\
0 & 0
\end{bmatrix} U(k) + \begin{bmatrix} 1\\0\\0\\1\\0\\0 \end{bmatrix} \tilde{r}(k).
\end{aligned}
\tag{5}
$$

Here, $\tilde{r}(k)$ is functioned as the feedforward part to trim the setpoints. The state space representation is

$$
X(k+1) = FX(k) + GU(k) + E\tilde{r}(k),
\tag{6}
$$

where

$$
F = \begin{bmatrix}
-(a_{11}+a_{12}) & 1 & 0 & 0 & 0 & 0\\
-(a_{11}a_{12}) & 0 & 0 & 0 & 0 & 0\\
1 & 0 & 1 & 0 & 0 & 0\\
0 & 0 & 0 & -(a_{21}+a_{22}) & 0 & 0\\
0 & 0 & 0 & -(a_{21}a_{22}) & 0 & 0\\
0 & 0 & 0 & 1 & 0 & 1
\end{bmatrix},
$$

$$
G = \begin{bmatrix}
-b_{11} & -b_{12}\\
-b_{11}a_{12} & -b_{12}a_{11}\\
0 & 0\\
-b_{21} & -b_{22}\\
-b_{21}a_{22} & -b_{22}a_{21}\\
0 & 0
\end{bmatrix}, \text{and } E = \begin{bmatrix} 1\\0\\0\\1\\0\\0 \end{bmatrix}.
\tag{7}
$$

For PID control law, it is the linear combination of two error states $e(k-1)$, $e(k)$ and one integrator state $\theta(k)$. Let's define the PID state vector

$$
\tilde{X}(k) = \begin{bmatrix} e_1(k) \\ e_1(k-1) \\ \theta_1(k) \\ e_2(k) \\ e_2(k-1) \\ \theta_2(k) \end{bmatrix}.
\tag{8}
$$

The relationship between $X\tilde{(}k)$ and $X(k)$ is

$$
X(k) = M\tilde{X}(k) + NU(k-1)
\tag{9}
$$

where

$$
M = \begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0\\
0 & -(a_{11}a_{12}) & 0 & 0 & 0 & 0\\
0 & 0 & 1 & 0 & 0 & 0\\
0 & 0 & 0 & 1 & 0 & 0\\
0 & 0 & 0 & 0 & -(a_{11}a_{12}) & 0\\
0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
$$

$$
\text{and } N = \begin{bmatrix}
0 & 0\\
-b_{11}a_{12} & -b_{12}a_{11}\\
0 & 0\\
0 & 0\\
-b_{21}a_{22} & -b_{22}a_{21}\\
0 & 0
\end{bmatrix}.
$$

The GPC cost function is defined as

$$
\begin{aligned}
J = \sum_{l=1}^{p} \big[&X(k+l)^T Q_l X(k+l)\\
&+ U(k+l-1)^T R_l U(k+l-1) \big]
\end{aligned}
\tag{10}
$$

The future outputs $X(k+l)$ can be obtained recursively as

$$\begin{aligned} X(k+1) &= FX(k) + GU(k) + E\tilde{r}(k) \\ X(k+2) &= F^2X(k) + FGU(k) + GU(k+1) \\ &\quad + FE\tilde{r}(k) + E\tilde{r}(k+1) \\ &\quad \vdots \\ X(k+l-1) &= F^{l-1}X(k) + F^{l-2}GU(k) \\ &\quad + F^{l-3}GU(k+1) + \cdots + GU(k+l-2) \\ &\quad + F^{l-2}E\tilde{r}(k) + F^{l-3}E\tilde{r}(k+1) + \dots \\ &\quad + E\tilde{r}(k+l-2) \\ X(k+l) &= F^{l}X(k) + F^{l-1}GU(k) \\ &\quad + F^{l-2}GU(k+1) + \cdots + GU(k+l-1) \\ &\quad + F^{l-1}E\tilde{r}(k) + F^{l-2}E\tilde{r}(k+1) + \dots \\ &\quad + E\tilde{r}(k+l-1) \end{aligned} \quad (11)$$

Augmenting these system response into stacked vectors,

$$\bar{X} = HFX(k) + P\bar{U} + \bar{E}\tilde{R}, \quad (12)$$

where

$$\bar{X} = \begin{bmatrix} X(k+1) \\ X(k+2) \\ \vdots \\ X(k+l-1) \\ X(k+l) \end{bmatrix}, \; \bar{U} = \begin{bmatrix} U(k) \\ U(k+1) \\ \vdots \\ U(k+l-2) \\ U(k+l-1) \end{bmatrix},$$

$$\tilde{R} = \begin{bmatrix} \tilde{r}(k) \\ \tilde{r}(k+1) \\ \vdots \\ \tilde{r}(k+l-2) \\ \tilde{r}(k+l-1) \end{bmatrix}, \; P = \begin{bmatrix} G & 0 & \dots & 0 \\ FG & G & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots \\ F^{l-1}G & F^{l-2}G & \dots & G \end{bmatrix},$$

$$H = \begin{bmatrix} I \\ F \\ \vdots \\ F^{l-1} \end{bmatrix}, \text{ and } \bar{E} = \begin{bmatrix} E & 0 & \dots & 0 \\ FE & E & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots \\ F^{l-1}E & F^{l-2}E & \dots & E \end{bmatrix}.$$

Substituting into Equation (13)

$$J = [HFX(k) + P\bar{U} + \bar{E}\tilde{R}]^T Q [HFX(k) + P\bar{U} + \bar{E}\tilde{R}] + \bar{U}^T R \bar{U}. \quad (13)$$

The unconstrained optimal condition is

$$\frac{\partial J}{\partial \bar{U}} = 2P^T Q([HFX(k) + P\bar{U} + \bar{E}\tilde{R}] + 2R\bar{U} = 0. \quad (14)$$

Thus, the optimal control sequence is given as

$$\bar{U} = -[P^T Q P + R]^{-1} P^T Q (HFX(k) + \bar{E}\tilde{R}). \quad (15)$$

Using the receding horizon philosophy, only the first control step is applied. Let's define

$$D = [I \;\; 0 \dots \; 0].$$

Thus, the control law is given by

$$U(k) = K_{GPC} X(k) + K_{ref} \tilde{R}. \quad (16)$$

where $K_{GPC} = -D[P^T Q P + R]^{-1} P^T Q H F$ and $K_{ref} = -D[P^T Q P + R]^{-1} P^T Q \bar{E}$.

The purpose of the proposed method is to find the way to design PID controller. Above control law is related to the state variable $X(k)$. We need convert it into the one related with $\tilde{X}(k)$. Replacing $X(k)$ in Equation (16) with Equation (9), it is obtained

$$U(k) = K_{GPC}(M\tilde{X}(k) + NU(k-1)) + K_{ref}\tilde{R}. \quad (17)$$

Thus, the final PID controller is

$$U(k) = K_{PID}\tilde{X}(k) + K_u U(k-1) + K_{ref}\tilde{R}, \quad (18)$$

where $K_{PID} = K_{GPC}M$ and $K_u = K_{GPC}N$.

3. TEMPERATURE CONTROL IN LITHOGRAPHY

In this paper, the proposed predictive ratio control is applied to thermal processing system in lithography (ITRS [2006]). Fig. 1 depicts the typical steps in a lithography process. This sequence of operations begins with a priming step to promote adhesion of the polymer photoresist material to the substrate. A thin layer of resist is spin-coated on the wafer surface. The solvent is evaporated from the resist by a baking process (softbake). After patterning with (deep UV) radiation, a post-exposure bake process is used to promote a reaction that alters the solubility of the resist in the exposed areas. A subsequent chemical develop step then removes the exposed/reacted resist material while keeping the non-exposed areas in place. The developed resist is then baked to promote etching stability.

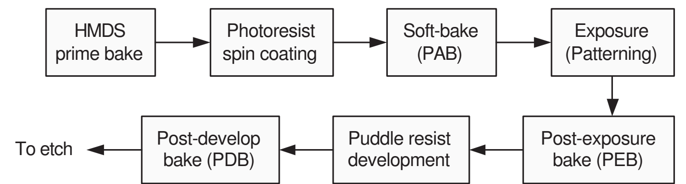

Fig. 1. Typical steps in the microlithography sequence.

As shown in Fig. 1, temperature control is critical in the lithography sequence. First, the PEB step is especially sensitive to temperature variation calling for precise temperature control. There are several areas where the performance of bake and chill plates can be improved. A number of recent investigations also show the importance of proper bake plate operation on CD control (Steele, et al. [2002], Hisai, et al. [2002]). For example, temperature nonuniformities during transients, including ramp-up and the movement of the substrate between the bake and chill plates, need to be minimized to narrow the CD distribution. To improve the transient and spatial control of the bake and chill plates a new approach to the design is needed. The reason is that the large thermal mass of the conventional hot plates prevents rapid movements in substrate temperature to compensate for real-time errors during transients. The implementation of advanced control systems with conventional technology cannot overcome the inherent operating limitations. We investigated this problem of PEB temperature control. Our approach was to modify the conventional technology so that the temperature nonuniformities during the transients could be controlled. This required consideration of the dynamics involved in wafer heating, as well as practical material and

operating issues to achieve repeatable and sustained operations. In addition, to improve the quality and throughput of the lithography process, one way is to incorporate several steps such as baking, chilling and spinning into an integrated system. The overall process time can be reduced if temperature can be controlled as the wafer is being spun at different speeds in readiness for the next step.

Figure 2 shows the proposed thermal processing system. The details are described in (Ho, et al. [2004]) and (Tay, et al. [2005]). The system integrates the baking and chilling steps into a single module, this eliminate undesirable temperature fluctuations and an uncontrolled situation due to substrate movement. The heater module is comprised of an array of heating zones that allow for spatial control of temperature in non-symmetric configurations. Each of the heating zones is separated by an air-gap of approximately 200 μm. A resistive heating element is embedded within each of the heating zones. Each heating zone is configured with its own temperature sensor and electronics for feedback control. Multivariable feedback control algorithms are used to manipulate the heating zones to the desired substrate temperature profile. A chill plate circulating water is used to remove heat from the base plate, and the connected heating elements. The system also provides in-situ sensing of the substrate temperature. During baking, the substrates rest on proximity pins which has temperature sensors embedded in it. Real-time closed-loop control of the substrate temperature is thus possible as oppose to conventional open-loop control of the substrate temperature. Its small thermal mass allows for fast dynamic manipulation of temperature profile. Depending on application, the number of zones of the bake-plate can be easily configured.

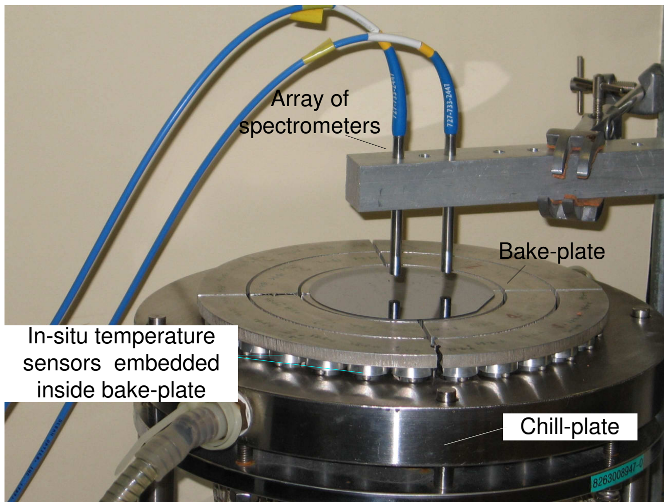

Fig. 2. Integrated multizone bake/chill module.

3.1 *Modeling of multizone thermal system*

In this section, we will only present the system dynamics for a 2-zone system shown in Fig. 3. Spatial distributions of temperature and other quantities in a silicon wafer are most naturally expressed in a cylindrical coordinate system. We will assume that the substrate used for baking is a silicon wafer and the bake-plate is cylindrical in shape with the same diameter as the wafer. Energy balances on the wafer and bake-plate for the simplified 2-zone system can then be carried out to obtain a two dimensional model as follows.

$$C_{p1}\dot{T}_{p1} = -\frac{T_{p1}-T_{p2}}{R_{p1}} - \frac{T_{p1}-T_{w1}}{R_{a1}} + q_1 \tag{19}$$

$$C_{p2}\dot{T}_{p2} = \frac{T_{p1}-T_{p2}}{R_{p1}} - \frac{T_{p2}}{R_{p2}} - \frac{T_{p2}-T_{w2}}{R_{a2}} + q_2 \tag{20}$$

$$C_{w1}\dot{T}_{w1} = \frac{T_{p1}-T_{w1}}{R_{a1}} - \frac{T_{w1}-T_{w2}}{R_{w1}} - \frac{T_{w1}}{R_{wz1}} \tag{21}$$

$$C_{w2}\dot{T}_{w2} = \frac{T_{w1}-T_{w2}}{R_{w1}} + \frac{T_{p2}-T_{w2}}{R_{a2}} - \frac{T_{w2}}{R_{w2}} - \frac{T_{w2}}{R_{wz2}} \tag{22}$$

where T_{p1} and T_{p2} are the zone 1 and zone 2 bakeplate temperature above ambient; T_{w1} and T_{w2} are the zone 1 and zone 2 wafer temperature above ambient; C_{p1} and C_{p2} are the thermal capacitance of zones 1 and 2 of bakeplate elements; C_{w1} and C_{w2} are the thermal capacitance of zones 1 and 2 of wafer elements; R_{p1} is the thermal conduction resistance between zone 1 and zone 2 of bakeplate elements; R_{p2} is the thermal convection loss of zone 2 bakeplate element in the radial direction; R_{w1} is the thermal conduction resistance between zone 1 and zone 2 of wafer elements; R_{w2} is the thermal convection loss of zone 2 wafer element in the radial direction; R_{wz1} and R_{wz2} are the thermal convection loss of zone 1 and 2 of wafer in the z direction; R_{a1} and R_{a2} are the thermal conduction resistance between bakeplate and wafer elements of zone 1 and 2; and q_1 and q_2 are the power into bakeplate zone 1 and 2. The detailed thermophysical properties can be found in (Ho, et al. [2004]).

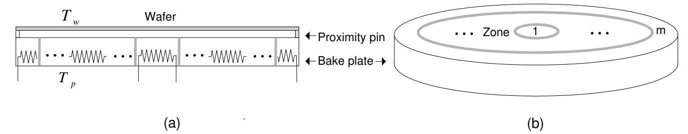

Fig. 3. Thermal modeling of a m-zone thermal processing system. For a 2 zone system, m=2 corresponds to the outer zone.

The relationship between the steady state wafer temperature and bakeplate temperatures for the two zone thermal system can be obtained from (22) as

$$T_{p1}(\infty) = R_{a1}\left(\frac{1}{R_1}T_{w1}(\infty) - \frac{1}{R_{w1}}T_{w2}(\infty)\right) \tag{23}$$

$$T_{p2}(\infty) = R_{a2}\left(\frac{1}{R_2}T_{w2}(\infty) - \frac{1}{R_{w1}}T_{w1}(\infty)\right), \tag{24}$$

where

$$R_1 = \frac{1}{\frac{1}{R_{a1}} + \frac{1}{R_{w1}} + \frac{1}{R_{wz1}}}$$

and

$$R_2 = \frac{1}{\frac{1}{R_{w1}} + \frac{1}{R_{a2}} + \frac{1}{R_{w2}} + \frac{1}{R_{wz2}}}.$$

Equations (23) and Equations (24) show the required temperature set-points for the bakeplate to achieve the desired steady-state wafer temperature and spatial temperature uniformity. In this way, the relationship between the wafer and bakeplate temperature at the steady state can be obtained from the physical modeling of the baking process. The corresponding bakeplate temperature can

be controlled to achieve the desired steady state wafer temperature.

4. SIMULATION RESULTS

In this section, the simulation results are presented. The GPC-based PID controller is designed to control the bakeplate temperature to achieve wafer temperature uniformity. The setpoints for the two zone bakeplate temperatures are set to be different values. The different setpoints for bakeplate temperatures are obtained with the steady-state relationship between wafer and bakeplate temperatures according to Equations (23) and (24). In the example, the desired steady-state wafer temperatures of zone 1 and 2 are set to be $90°C$. Therefore, the setpoints for bakeplate are calculated as $93.15°C$ and $93.8076°C$ for zone 1 ans 2 respectively. When the ratio control is applied, we set the ratio $\alpha = y_{1d}/y_{2d} = 93.15/93.8076 = 0.993$, where y_{1d} and y_{2d} are the desired outputs of the bakeplate temperatures respectively. Before the proposed method is implemented, the process model needs to be identified first with the open loop step response. The identified model is obtained as

$$Y_1(s) = \frac{1.6749}{484.705s+1}U_1(s) + \frac{1.337}{614.52s+1}U_2(s) \quad (25)$$

$$Y_2(s) = \frac{1.337}{614.52s+1}U_1(s) + \frac{1.4476}{567.08s+1}U_2(s), \quad (26)$$

where $y_1(t)$ and $y_2(t)$ are the bakeplate temperatures of zone 1 and zone 2; $u_1(t)$ and $u_2(t)$ are corresponding power input into zone 1 and 2. In the simulation study, the sampling time used is 0.5s. The PID controller are designed according to the proposed approach. K_{PID} is derived to be

$$K_{PID} = \begin{bmatrix} 66.5833 & -38.4779 & 0.1316 & 19.6511 & -6.1457 & 3.7310 \\ 329.2707 & -186.8232 & 0.7386 & 479.1656 & -168.2897 & 73.9261 \end{bmatrix}.$$

Here, in the ratio control, the output y_2 is multiplied by α and it is adopted as the setpoint of bakeplate zone 1, i.e. $r_1(t) = \alpha y_2(t)$, i.e., let y_1 follows y_2. This is reasonable since $y_2(t)$ exhibits a more sluggish response than $y_1(t)$. This structure is effectively one of series ratio control which can reduce the influence from the load disturbance. Another configuration is the parallel ratio control which uses independent setpoints, i.e., $r_1 = \alpha r_2$. In this section, results from the two kinds of ratio control will be compared.

Figure 4 shows the setpoints for the two-zone thermal system with ratio control, $r_1 = \alpha y_2$. Incorporating with the feature of ratio control, the simulation results are presented. Figure 5 shows the bakeplate temperatures of two zones. Figure 6 shows the wafer temperatures and the nonuniformity. Here it can be seen that the maximum wafer temperature nonuniformity is $0.7479°C$ in the transient response and $-0.0079°C$ in the steady state.

As a comparison, the parallel ratio control, $r_1 = \alpha r_2$, are presented. Figure 7 shows the responses of the bakeplate temperatures and the corresponding setpoints with ratio

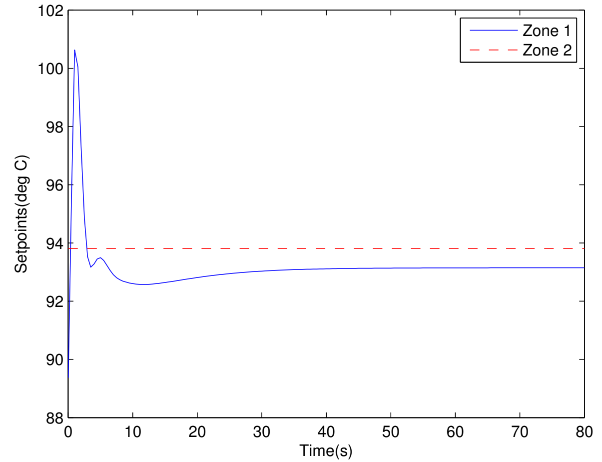

Fig. 4. Setpoints with ratio control, $r_1 = \alpha y_2$

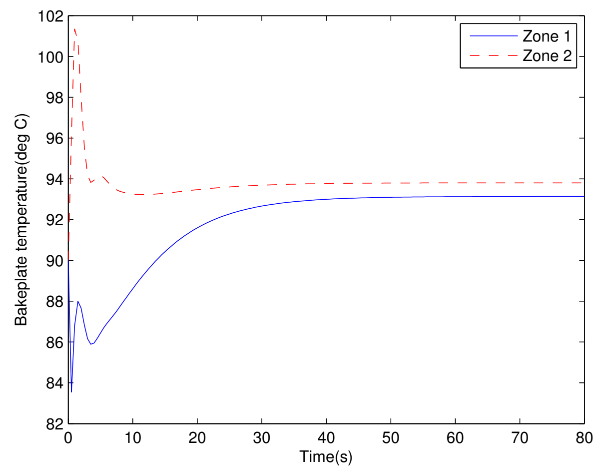

Fig. 5. Bakeplate temperatures with ratio control, $r_1 = \alpha y_2$

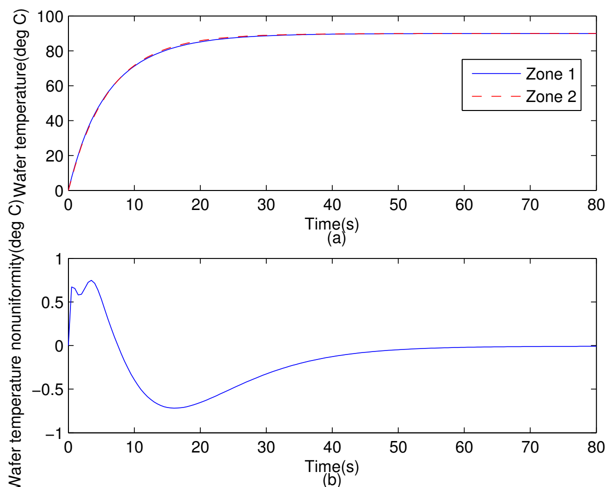

Fig. 6. Wafer temperature and nonuniformity with ratio control, $r_1 = \alpha y_2$ (a). Wafer temperature (b). Wafer temperature nonuniformity

control. Figure 8 shows the wafer temperatures and the nonuniformity. Under the predictive parallel ratio control, the maximum wafer temperature nonuniformity is $0.9322°C$ during the transient state and $-0.0069°C$ in the steady state. Compared to the parallel ratio control, the series ratio control, $r_1 = \alpha y_2$, has good performance in the transient response.

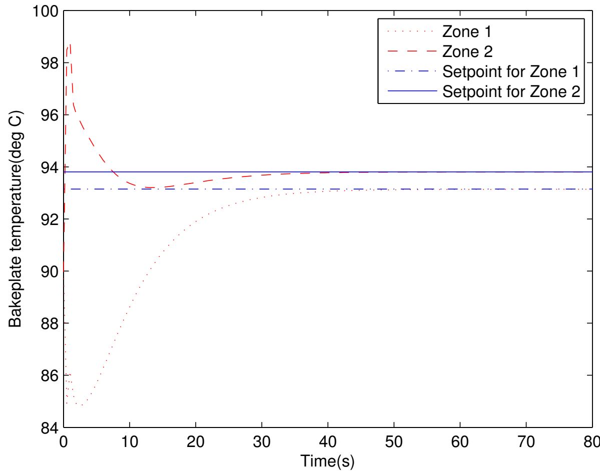

Fig. 7. Bakeplate temperatures and the setpoints with ratio control, $r_1 = \alpha r_2$

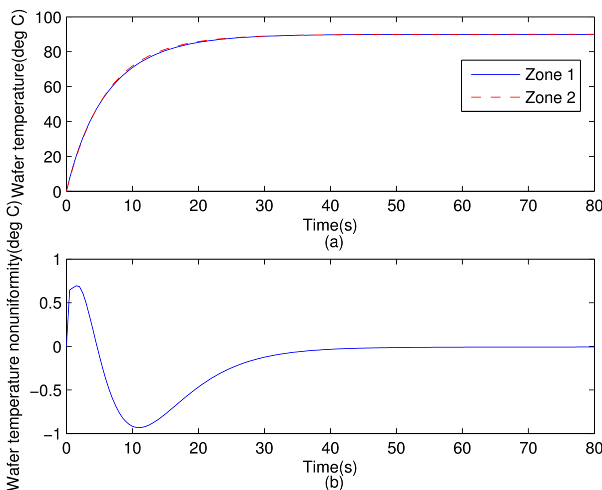

Fig. 8. Wafer temperature and nonuniformity with ratio control, $r_1 = \alpha r_2$ (a). Wafer temperature (b). Wafer temperature nonuniformity

5. CONCLUSION

We present the development of a ratio control strategy for controlling spatial temperature uniformity of a silicon wafer substrate. Our approach takes into consideration the interaction between the different heating zone of the novel multizone thermal system. The detailed thermal modeling of the system is analyzed based on first principle heat transfer. Based on the model, simulations are carried out to verify the feasibility of the system. The resultant model-based GPC PID controller is simulated on the multizone thermal system. Simulation results shows that spatial temperature uniformity can be controlled to within 1^oC and 0.1^oC during transient and steady-state operating condition respectively.

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