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Towards MiroSot Robots with FPGA- and DSP-based Image Processing On-Board

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Abstract: Fast self-location and collision-free navigation is a crucial pre-requisite for autonomous robots in real-world environments. Usually robots are equipped with a variety of sensors, but for obvious reasons vision systems are by far the most informative and reliable source for object location and path planning. In this paper, we present a new DSP- and FPGA-based image processing system for FIRA MiroSot robots endowed with 4 local VGA cameras. The use of FPGAs to link and pre-process camera data allows an enormous flexibility with regard to the number and type of cameras used. This kind of miniaturization for a processing system, as well as the low cost of components, can open new applications for image processing systems.

1. INTRODUCTION

Fast self-location and collision-free navigation is a crucial pre-requisite for autonomous robots in real-world environments. Robots usually have access to a variety of sensors, but for obvious reasons vision systems are by far the most informative and reliable source for (self-)location and path planning.

Robot soccer is an excellent test-bed to fathom new concepts for autonomy and vision systems. When it comes to autonomy in robot soccer, the field is quite diverse. Some leagues use non- or semiautonomous robots controlled by host computers and centralized vision, some use fully autonomous robots with local vision, some use intermediate designs. Generally speaking, the degree of autonomy mostly depends on the size of the robots. In turn, the speed of the game depends on the degree of autonomy (Weiss 2004).

The FIRA MiroSot league (FIRA 2007), one of 6 different categories that make up FIRA community, is characterized by the robots' remarkably high speed of up to 4 m/s. With 11 team players, the competition scenario resembles real-world soccer while posing an extraordinary challenge to the image processing systems.

In the MiroSot league, the information delivered by the overhead cameras at a height of 2.5 m (Middle League) or 3 m (Large League) above the field and a host PC running the image processing software are currently the only reliable data sources supporting the self-location process and the identification of lines and marks, the ball and the other robots. With a robot size strictly confined to a maximum of 7.5 cm on all sides, a centralized vision approach has been the only option for many years (Kim 2004). This setting has significantly restricted the autonomy of the robots, and it is evident that robots with local vision capabilities could propel the competitions to new levels of complexity.

This paper presents a new DSP- and FPGA-based image processing system for MiroSot robots endowed with 4 local VGA cameras. Five sub-tasks were addressed:

- Design of an FPGA-endowed board
- VHDL-programming of the FPGA
- Control of four camera modules and image pre-processing by the FPGA
- Communication between DSP und FPGA
- Image Processing on the DSP.

2. HARDWARE AND IMAGE PROCESSING WORKFLOW

2.1 The DROIDS3 Platform

Since 2001, the Chair Computer Science I at the University of Dortmund has designed and built his own robots. Currently, the 3rd generation, the DROIDS3 robots with an optimized mechanical design are being used. These robots with a maximum speed of 2.9 m/s feature also a stronger motor, a lithium-polymer battery and a completely re-designed DSP main board. The transfer of a part of the path-planning calculation from the host PC to the robot led to greater autonomy and opens up further research perspectives. From the beginning, the question whether it will be possible to implement a local high-performance image processing system that makes use of the DSP's processing power was an challenging idea (Dortmund Droids 2006).

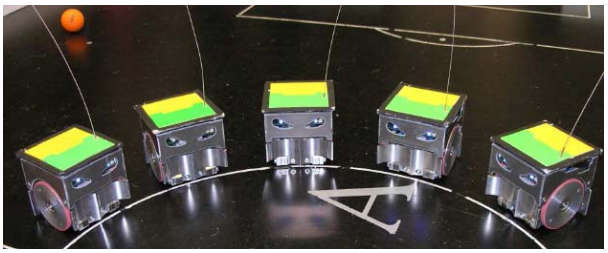

Fig. 1. DROID3-Robots: tracking module in image processing system allows only two colours

2.2 Image Processing Workflow

The typical centralised image processing workflow – from pixel classification to decision-making capabilities in terms of positions and movements of the objects on the field – is outlined in Fig. 2 (Weiss 2003, Weiss et.al. 2004). Basically, this sequence of steps has to be transferred from the global scenario to a local image-processing system.

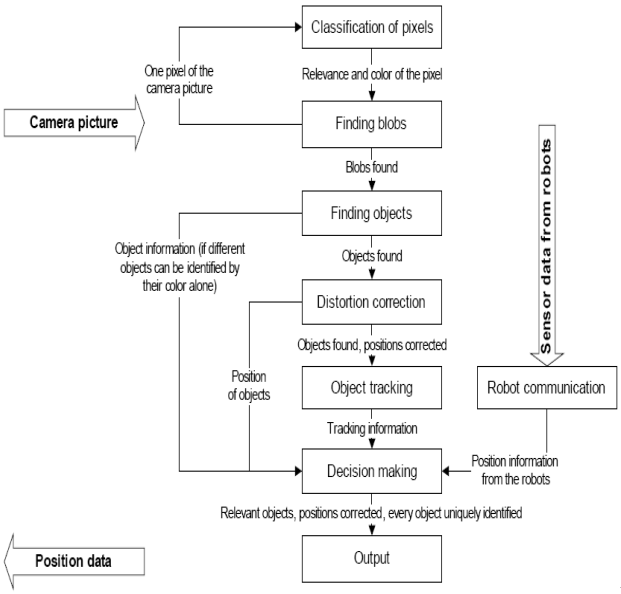

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Fig. 2: Modules of the recognition process with data flow (simplified)

3. HARDWARE CONFIGURATION

The local vision system's main hardware components include the DSP on the mainboard, the FPGA, a four-layer board, and the camera modules (Schulz 2006).

3.1 DSP and Main Board

The central module of the DROID3 main board (Fig. 3) is the TI TMS320f2812 DSP. This 32-bit DSP performs a clock rate of 150 MHz, although its effective performance depends on a number of conditions. When the board was designed some years ago, extension slots were already considered to be able to connect the DSP mainboard with a dedicated local vision board.

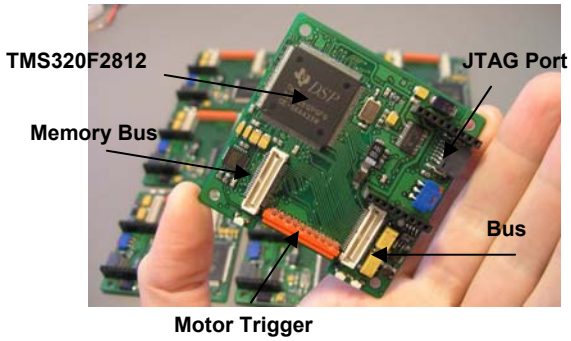

Fig. 3. DSP main board of the DROIDS3 generation

3.2 FPGA Chip and Board

The preferred FPGA is a Xilinx Spartan-3 featuring specific characteristics: 400,000 system gates, 896 configurable logic blocks (CLBs), up to 56KBits distributed RAM, up to 288 KBit RAM, 16 complete 18x18-bit multipliers, and four digital clock managers.

This device is a SRAM-based FPGA, i.e. the configuration data have to be reloaded onto the FPGA after a reset. Three different procedures would be possible, but in this instance we choose a seriel platform Flash PROM. This Xilinx Platform Flash PROM XCF04SV has a storage capacity of 4 MBit and a serial interface, connecting it with the FPGA. While applying the supply voltage, the configuration stored on the Flash PROM is transferred to the FPGA.

The FPGA is fixed on a four-layer board (Fig. 4), although a six-layer board would be preferable. Most of the components are located on the first layer. The second and the third layer accommodate the signal wires, as well as most of the voltage pcb track. The fourth layer, respectively the bottom side, features the plug-in connectors for the camera, flat ribbon cables and an interface to connect the FPGA board to the DSP board.

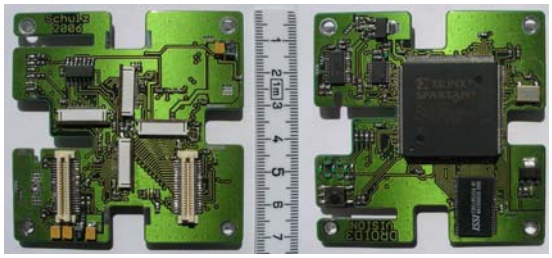

Fig. 4. DROID3vision board: lover and upper side

3.3 Camera Module

The Camera modules are Agilent ADCM-2700 CMOS units (Fig. 5). They have a freely configurable resolution of up to 640 x 480 pixels with 25.5 fps. The configuration is supported by an I^2C[14] bus and features specific options like image size, frame rate and automatic brightness adjustment. Each of the four cameras is connected separately to the FPGA.

Fig. 5. Agilent ADCM-2700 Camera Module

The cameras use three control signals to synchronise the image data. Following the FPGA configuration, all four camera modules are activated and configured simultaneously.

To be able to develop a cost-efficient prototype, all hardware components were selected with a view to their availability in small quantities.

DSP mainboard and DROID3vision FPGA board are jointly connected via two 40-pin interfaces.

4. VHDL IMPLEMENTATION

The FPGA is "configured" using the hardware programming language VHDL. The VHDL implementation is separated into a number of logically different modules. Fig. 6 outlines the modularised structure of the implementation. In addition, there are external interfaces connecting the DSP board, cameras and SRAM.

The core module of the implementation is the camera controller. This controller communicates with the other modules and pre-processes the images.

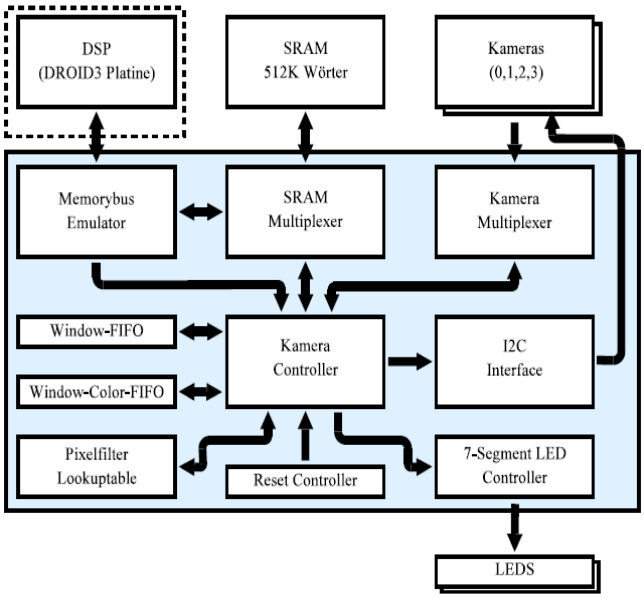

Fig. 6. Block Diagram of the VHDL-Implementation

The main tasks of the camera controller include edge detection and colour classification of the pixel data. To emphasise the edges, the incoming RGB555 pixel data are filtered by means of a low-pass filter, converting them into different shades of grey. Then a 5 x 5 Sobel operator is used to identify the edges. In addition, a look-up table pixel filter assigns the RGB555 data to one of 16 colours (see chapter 5).

Relevant modules of the FPGA implementation include:

- a I^2C master for the configuration of the Agilent cameras
- a window FIFO that is responsible for the edge detection
- a window colour FIFO to low-pass filter incoming pixel data
- a camera multiplexer to switch between cameras and synchronise their work and
- a memory bus emulator, which enables the FPGA from the perspective of the DSPs to act as a SRAM module.

The FPGA is connected to the DSP's external storage bus to facilitate fast access to the image data. The DSP reads in the information from the data bus with a simple mechanism, guaranteeing an easy and fast data transfer between DSP and FPGA.

5. IMAGE PROCESSING ON THE FPGA

Since the robot soccer project was launched at the University of Dortmund, numerous algorithms to classify colours and identify objects have been tested. The currently preferred algorithm classifies pixels using the Euclidean distance in the RGB colour space.

The straightforward implementation of a fast colour classification algorithm on the FPGA would require too many FPGA resources. Therefore, an efficient solution is indispensable. Considering that the cameras deliver only image data in RGB555 format, a look-up table to distinguish between up to 16 colours was introduced. The initial generation of the look-up table is performed on a PC and can be calculated by applying user-defined algorithms. The implementation of this look-up table requires less than 2% of the FPGA's resources.

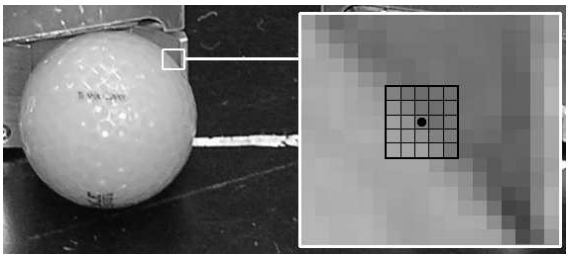

Fig. 7. 5 x 5 pixel window around an image point

The heart of the FPGA's edge detection capability is the window FIFO implementation of the Sobel operator. The computation is based on a 5 x 5-pixel window. The calculation of the 5 x 5 Sobel operators for each pixel occurs in real-time, taking up only an additional 4% of the FPGA's resources.

6. IMPLEMENTATION ON THE DSP

The DSP controls the access to the FPGA and operates the image processing. The image processing is based on a software modules for colour space and object recognition:

- Colour space recognition

  Starting point are the low-pass-filtered and colour-classified images as supplied by the FPGA and stored in the SRAM. The colour classification function takes these images and conducts a simple region-growing algorithm, optimised for short runtimes and as few pixels as possible. Then the centre of the space, as well as width and height of the colour spaces are defined – for up to 20

colour spaces. Initially, only every 8th pixel of the 640 x 649-pixel image is assessed. If a colour class other than black is detected, the actual search algorithm is initiated.

- Object recognition

The 20 colour space elements are the starting point. Starting with this list, a search to match known objects is initiated.

Each goal is defined by two coloured spaces – blue and green. Both areas are positioned at a distance of exactly 10 cm, and a blue area underneath the green one identifies the team's own goal. The distance to the goal is calculated on the basis of these pairs of colour markers and the distance between the colours. The use of two-coloured areas with a defined distance to each other makes the system significantly more robust in terms of a false recognition compared to a system with only one colour. When the goal markers are successfully recognised, the position of the robot and the alignment on the field are calculated

The ball is identified by the colour class "red". The calculation of the distance is based on the width of the colour area and reference data (calibration). The alignment of the ball with respect to the robot is calculated on the basis of the x-position in the image. To determine the position of the ball, it is necessary to identify the robot's own position. For this, all four camera images are analysed. The ball position is calculated on the basis of the robot's position and the angle to the robot.

7. RESULTS

A graphical user interface implemented on the robot allows taking different test scenarios into consideration. Some of these test scenarios will be presented on video during the presentation of this paper.

At first, a number of tests have been conducted to evaluate the quality of the FPGA/DSP-based image processing system. Initially, still images taken from the FPGA were analysed with respect to their quality.

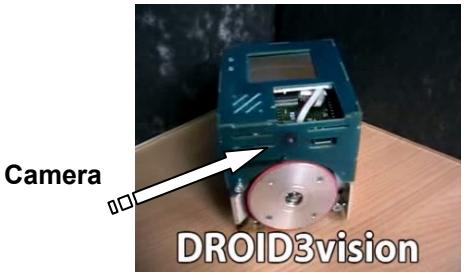

Fig. 8. Completely assembled DROID3vision Robot

The next step involved testing the precision of the self-location on 96 points on the field. As these tests were encouraging in the final analysis, three standard robot soccer situations were implemented on the robot:

- Take goalkeeper's position
- Attack
- Hold ball

Take goal position:

- Detect the team's own goal and start moving towards the goal until it is no longer captured by the image.
- Search for the opponent's goal, turn until the goal is in central focus of the side camera, and drive in a circular movement towards the centre of the field.
- Turn around so that the opponent's goal is in the central focus of the camera at the back.
- Move in a straight line towards the team's own goal and stop at a defined distance from the goal line.

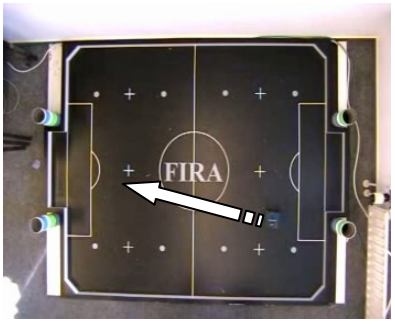

Fig. 9. Still picture "Take goal position"

Attack:

An attack is executed in four steps:

- The positions of the robot and the ball are calculated, the robot moves towards the ball and stops at a distance of 18 cm in front of the ball.
- The robot makes a 90-degree turn, surrounding the ball in a circle until reaching the right angle and making another 90-degree turn.
- Following an alignment adjustment towards the centre of the ball, the shot at the goal is initiated at high velocity.

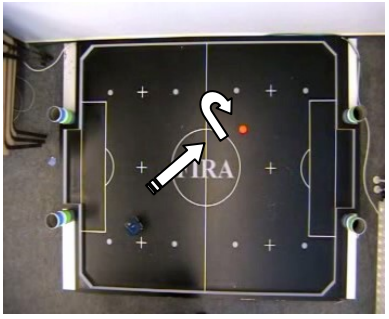

Fig. 10. Still picture "Attack"

- Having collided with the ball, the robot moves a certain distance before stopping.

Hold ball:

- As the ball is moving on the field towards the team's own goal, the robot moves on the same y coordinate.

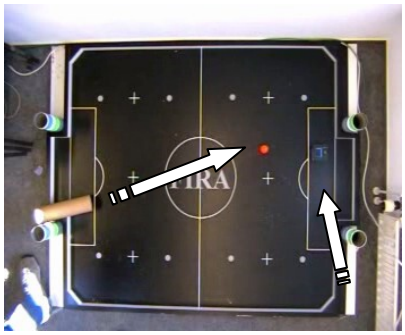

Fig. 11. Test picture "Hold ball"

8. CONCLUSIONS

The tests demonstrate that this image processing system supports a reliable self-location capability of the robots, a fast recognition of objects, and an excellent navigation, hence enabling autonomous, i.e. host-independent action. From a strategical viewpoint it could make sense to consider an A(utonomous) MiroSot league, as has been proposed by (Krywult et.al. 2006).

Furthermore, the miniaturisation of this image processing system featuring low-budget components opens new application fields and will demonstrate that it is possible to use these construction principles to develop low-cost, high-performance camera systems, which will be relevant for a variety of domains.

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