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Frequency Domain Based Repetitive Control of Three Phase Boost PWM Rectifier Under Distorted Supply Voltage Conditions

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Abstract: This paper presents a digital plug-in frequency domain based repetitive control scheme for minimizing the even order harmonics at the output dc link voltage and odd order harmonics in the line currents under the distorted and unbalanced supply voltage conditions. The proposed current controller consists of a conventional PI controller and a frequency domain based plug-in repetitive controller. Based on the mathematical model of the three-phase PWM boost rectifier under the generalized supply voltage conditions, the control task is divided into: (a) *dc-link voltage harmonics control* and (b) *line side current harmonics control*. The plug-in repetitive controller is designed to achieve line side currents with low THD for the three phase PWM boost rectifier. The repetitive control learning algorithm is designed in frequency domain instead of commonly used time domain and provides the flexibility of choosing different learning gains and phase delay compensations individually for each harmonic component. The experimental test results obtained from a 1.6 kVA laboratory based PWM rectifier confirm that the THD of the line side current can be reduced from 21.09% to 4.12% with the insertion of the plug-in frequency domain based repetitive controller.

Keywords: Nonlinear system control; Power converters; Modelling; Repetitive controller; Frequency domain design.

1. INTRODUCTION

Since the three phase boost PWM rectifier offers the possibility of low line side current distortions with unity power factor operation and constant dc-link voltage with a small output filter capacitor, it has increasingly been employed for high-performance applications such as adjustable-speed drives (ASD), uninterruptible power supplies (UPS) in recent years. However, all the advantages of the PWM boost rectifier are valid only with the assumption of balanced input supply voltage conditions. Nevertheless, the unbalanced and distorted input supply voltage conditions occur frequently in real life situation, particularly in a weak ac system. EN 50160 [1994] standard allows 6% low order supply voltage harmonics, and supply voltage sags/swells within ±10%. The unbalanced supply voltages which cause the negative sequence and the harmonic component voltage in the supply voltages would deteriorate the performance of the PWM rectifier. Rioual et al. [1996] have shown that the unbalanced input supply voltages lead to the appearance of even order harmonics at the dc output and odd order harmonics in the input line currents. Also, Wu et al. [2007] have proven that the distorted supply voltages cause the corresponding odd order harmonics in the supply line side currents. Therefore, high performance of the PWM rectifier should be ensured even under such varying and unbalanced supply voltage conditions.

Extensive studies have been carried out to investigate the influence of the unbalanced input supply voltages on the output dc link voltage. And many control schemes have been proposed to eliminate the even order harmonics at the dc output voltage such as Song and Nam [1999], Stankovic and Lipo [2001], Suh et al. [2002], Wu et al. [2006]. Consequently, the harmonics in the ac line currents can be eliminated as a side effect. Therefore, when the supply voltages are distorted, those control schemes can hardly handle the current harmonics on the supply side. In this paper, a hybrid frequency domain based repetitive control (FDRC) scheme is proposed to effectively minimize the line side current harmonics and the dc link voltage harmonics under the distorted and unbalanced operating conditions. Based on the mathematical model (see Wu et al. [2006]) of the three-phase PWM boost rectifier in the positive and negative synchronous rotating frames, the control objectives can be separated as *voltage harmonics control* and *current harmonics control*. A plug-in FDRC is designed and employed in *current harmonics control* scheme to eliminate the current harmonics in the line side. The learning algorithm in FDRC uses Fourier series analysis to obtain the different magnitude and phase angle of each chosen frequency component, and utilizes these information to reconstruct a signal for learning process. As a result, the low THD line side currents of the three phase PWM boost rectifier under the distorted supply voltage

conditions can be achieved. The experimental test results provided validate the effectiveness of the proposed control scheme on a 1.6 kVA laboratory based three phase PWM rectifier.

2. MODELING OF THREE PHASE BOOST PWM CONVERTER

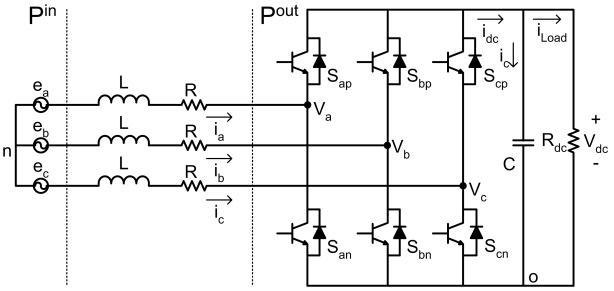

Fig. 1. Three phase PWM AC-DC boost rectifier circuit

Fig. 1 shows the power circuit configuration of a three phase PWM AC-DC boost rectifier. It is assumed that the converter is feeding a resistive load. If zero-sequence voltage is assumed to be absent, then the system can be resolved into the positive and negative rotating space vectors in the synchronous frame, respectively. Therefore, the model of the line currents can be expressed in the positive and negative rotating synchronous d-q frame as Rioual et al. [1996],

$$\begin{bmatrix} \dot{i}_d^p \\ \dot{i}_q^p \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega \\ -\omega & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_d^p \\ i_q^p \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} e_d^p \\ e_q^p \end{bmatrix} + \begin{bmatrix} -\frac{v_{dc}}{L} & 0 \\ 0 & -\frac{v_{dc}}{L} \end{bmatrix} \begin{bmatrix} S_d^p \\ S_q^p \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} \dot{i}_d^n \\ \dot{i}_q^n \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\omega \\ \omega & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_d^n \\ i_q^n \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} e_d^n \\ e_q^n \end{bmatrix} + \begin{bmatrix} -\frac{v_{dc}}{L} & 0 \\ 0 & -\frac{v_{dc}}{L} \end{bmatrix} \begin{bmatrix} S_d^n \\ S_q^n \end{bmatrix} \tag{2}$$

where the variables e, i and S represent the supply voltage, current and average switching function, respectively. Superscripts p and n designate the positive-sequence and the negative-sequence, respectively, and subscripts α and β represent the variables in the stationary α-β frame, and d and q represent the same in the rotating d-q frame.

Considering that the dc link voltage v_{dc} is almost constant because of the relatively small ripple, the state space model described by Eqns.(1) and (2) has a linear characteristic. Hence, under the distorted supply voltages e_a, e_b and e_c, if the control signals S_d^p, S_q^p, S_d^n and S_q^n are not able to completely compensate the harmonics in the voltages e_d^p, e_q^p, e_d^n and e_q^n, the corresponding harmonic components would appear in the currents i_d^p, i_q^p, i_d^n and i_q^n. Consequently, it would cause the odd order harmonics in the ac line currents i_a, i_b and i_c.

Finally, the dynamics of the dc link voltage can be presented as (see Wu et al. [2006]):

$$\begin{aligned} C\dot{v}_{dc} &= -\frac{1}{R_{dc}} v_{dc} + i_{dc} \\ &= -\frac{v_{dc}}{R_{dc}} + \begin{bmatrix} i_d^n \cos 2\theta + i_q^n \sin 2\theta + i_d^p \\ i_q^n \cos 2\theta - i_d^n \sin 2\theta + i_q^p \\ i_d^p \cos 2\theta - i_q^p \sin 2\theta + i_d^n \\ i_d^p \sin 2\theta + i_q^p \cos 2\theta + i_q^n \end{bmatrix}' \begin{bmatrix} S_d^p \\ S_q^p \\ S_d^n \\ S_q^n \end{bmatrix} \end{aligned} \tag{3}$$

The equation (3) gives the complete picture about the dc link voltage variation of the PWM rectifier. When it works under the ideal balanced operating condition, v_{dc} only contains the average dc quantity with all the negative sequence components being maintained at zero. While under the distorted and unbalanced operating conditions, it leads to the presence of the harmonic components and the negative sequence components both in currents as well as average switching function. Correspondingly, these components cause the even order harmonic components at the output of the rectifier as can be seen from the second term in (3).

3. CONTROL STRATEGY

The control objective to operate the three phase PWM rectifiers under the distorted and unbalanced supply voltage conditions can be highlighted as,

- to eliminate the even-order harmonics at the dc link voltage
- to eliminate the odd-order harmonics in the line side currents

Accordingly, the control signals S_d^p, S_q^p, S_d^n and S_q^n can be divided into two parts, 1) *voltage harmonics control signals*, S_{dv}^p, S_{qv}^p, S_{dv}^n and S_{qv}^n, those are used to take care of the even-order harmonics at the dc link voltage, and 2) *current harmonics control signals*, S_{di}^p, S_{qi}^p, S_{di}^n and S_{qi}^n, those are supposed to eliminate the odd-order harmonics in the line currents. (see Wu et al. [2007])

In *DC Link Voltage Harmonics Control* scheme, current harmonics control signals S_{di}^p, S_{qi}^p, S_{di}^n and S_{qi}^n can be ignored and voltage harmonics control signals, S_{dv}^p, S_{qv}^p, S_{dv}^n and S_{qv}^n, are mainly responsible to eliminate the even order harmonics at the dc link voltage. In *Line Side Current Harmonics Control* scheme, the effect from the supply voltage harmonics must be compensated by current harmonics control signals, S_{di}^p, S_{qi}^p, S_{di}^n and S_{qi}^n and the other part of control signals, S_{dv}^p, S_{qv}^p, S_{dv}^n and S_{qv}^n, are maintained constant to ensure the required line currents. The detailed implementation of the control strategy is discussed in the following sections.

3.1 DC Link Voltage Harmonics Control

In the steady-state condition, the variables at the dc side can be replaced by the sum of dc and ac signals as $v_{dc} = \overline{v_{dc}} + \Delta v_{dc}$ and $i_{dc} = \overline{i_{dc}} + \Delta i_{dc}$. The dc signals $\overline{v_{dc}}$ and $\overline{i_{dc}}$ are represented as the average value of the dc side

voltage and current. Considering that the contribution for *DC Link Voltage Harmonics Control* only comes from the voltage harmonics control signals, S^p_{dv}, S^p_{qv}, S^n_{dv} and S^n_{qv}, and the currents i^p_d, i^p_q, i^n_d, i^n_q are expected to be constant, the differential equation of the voltage model (3) can be solved easily. Finally, by neglecting the exponentially decaying term, the ac component of the dc link voltage can be derived as (4) according to Wu et al. [2006],

$$\Delta V_{dc} = \frac{R_{dc}\sqrt{M^2+N^2}}{\sqrt{1+4\omega^2C^2R^2_{dc}}}\sin(2\omega t+\phi_v) \tag{4}$$

where $M = -i^p_d S^n_{qv} + i^p_q S^n_{dv} + i^n_d S^p_{qv} - i^n_q S^p_{dv}$
$N = i^p_d S^n_{dv} + i^p_q S^n_{qv} + i^n_d S^p_{dv} + i^n_q S^p_{dv}$
$\cos\phi_v = \dfrac{R_{dc}(2C\omega R_{dc}N - M)}{\sqrt{(M^2+N^2)(1+4C^2\omega^2R^2_{dc})}}$

The amplitude of the second order harmonic term ΔV_{dc} is decided by the values of M and N. Therefore, only when the conditions, $M = 0$ and $N = 0$, are satisfied, the ac component of the dc link voltage is eliminated and a constant dc output voltage can be maintained. In the mean time, the input average active power P^{in}_o from the fundamental supply voltage determines the dc link voltage level and the average input reactive power Q^{in}_o decides the input power factor.

Therefore, the control laws can be expressed by a set of four linear equations in a matrix form as the following,

$$\begin{aligned}\begin{bmatrix} P^{in}_o \\ Q^{in}_o \\ M \\ N \end{bmatrix} &= \begin{bmatrix} P^{out}_o + P_{loss} \\ k_{pf}P^{in}_o \\ 0 \\ 0 \end{bmatrix} \\ &= \begin{bmatrix} e^p_{d1} & e^p_{q1} & e^n_{d1} & e^n_{q1} \\ e^p_{q1} & -e^p_{d1} & -e^n_{q1} & e^n_{d1} \\ S^n_{qv} & -S^n_{dv} & -S^p_{qv} & S^p_{dv} \\ S^n_{dv} & S^n_{qv} & S^p_{dv} & S^p_{qv} \end{bmatrix} \begin{bmatrix} i^{p*}_d \\ i^{p*}_q \\ i^{n*}_d \\ i^{n*}_q \end{bmatrix}\end{aligned} \tag{5}$$

where $k_{pf} = \frac{\sqrt{1-pf^2}}{pf}$, during the unity power factor operation, k_{pf} is equal to zero, and S^p_{dv}, S^p_{qv}, S^n_{dv} and S^n_{qv} are the switching signals obtained in the previous step.

The whole control block diagram of the cascaded dual frame current regulator with a voltage regulator is shown in Fig. 2. The reference input average active power P^{in}_o can be obtained from the outer voltage control loop. Then the estimation of the input average active power can be used in the reference current calculation according to (5). The current control calculation algorithm is implemented in the current reference calculating block of the control scheme to provide the four reference commands (i^{p*}_d, i^{p*}_q, i^{n*}_d, i^{n*}_q) for the inner current control loop. The inner loop is made up of two parallel positive and negative sequence *d-q* synchronous frame current regulators for each *d*- and *q*-axis.

3.2 Line Side Current Harmonics Control

In the power distribution networks, voltage distortions due to current harmonics is becoming a major concern because of the large numbers of nonlinear loads. Electronic power converters used in variable speed drives, SCR drives, etc., are the largest contributors to harmonic distortions. It is not uncommon to have current THD levels as high as 25% within some industrial settings as Bollen [1999].

The unbalanced and distorted three phase voltages e_a, e_b and e_c are composed of the positive sequence components e^p_a, e^p_b, e^p_c and the negative sequence components e^n_a, e^n_b, e^n_c. The positive sequence components can be written as the sum of kth-order harmonics with an amplitude E^p_k and angle offset angle θ^p_k in (6). The negative sequence components can also be expressed and analyzed in a similar way, but not elaborated here due to the space constraint.

$$\begin{aligned} e^p_a &= \sum_{\substack{n=1 \\ k=1,6n-1,6n+1}}^{\infty} E^p_k \sin(k\omega t+\theta^p_k) \\ e^p_b &= \sum_{\substack{n=1 \\ k=1,6n-1,6n+1}}^{\infty} E^p_k \sin(k\omega t - k\cdot\frac{2\pi}{3}+\theta^p_k) \\ e^p_c &= \sum_{\substack{n=1 \\ k=1,6n-1,6n+1}}^{\infty} E^p_k \sin(k\omega t + k\cdot\frac{2\pi}{3}+\theta^p_k) \end{aligned} \tag{6}$$

By using *Park's transformation* and *Clark's Transformation*, the supply voltages can be resolved as e^p_{dk} and e^p_{qk} in the rotating *d-q* frame as shown in Wu et al. [2007],

when $\mathbf{k = 1}$,

$$e^p_{d1} = \frac{\sqrt{6}E^p_1}{2}\sin\theta^p_1 \tag{7}$$

$$e^p_{q1} = -\frac{\sqrt{6}E^p_1}{2}\cos\theta^p_1 \tag{8}$$

$\mathbf{k = 6n\text{-}1}$,

$$e^p_{dk} = \frac{\sqrt{6}E^p_k}{2}\sin(6n\omega t+\theta^p_k) \tag{9}$$

$$e^p_{qk} = \frac{\sqrt{6}E^p_k}{2}\cos(6n\omega t+\theta^p_k) \tag{10}$$

$\mathbf{k = 6n{+}1}$,

$$e^p_{dk} = \frac{\sqrt{6}E^p_k}{2}\sin(6n\omega t+\theta^p_k) \tag{11}$$

$$e^p_{qk} = -\frac{\sqrt{6}E^p_k}{2}\cos(6n\omega t+\theta^p_k) \tag{12}$$

The equations (7)-(12) show that the fundamental voltages appear as constant voltage signals in the *d-q* frame, while the $(6n-1)$th and $(6n+1)$th order voltage harmonics result in the $6n$th order harmonics in the rotatory *d-q* frame. The corresponding $6n$th order harmonics would generate the harmonic currents of the same order in the rotating synchronous *d-q* frame (see Wu et al. [2007]). Consequently, this $6n$th order harmonics would reflect as the kth order harmonics in the *a-b-c* frame.

In practice, 5th, 7th, 11th and 13th order voltage harmonics are dominant in the power distribution networks. The above analysis indicates that under the generalized supply voltage conditions, the currents in the positive and negative rotating synchronous *d-q* frame consist of a dc component together with the 6th and 12th order harmonic

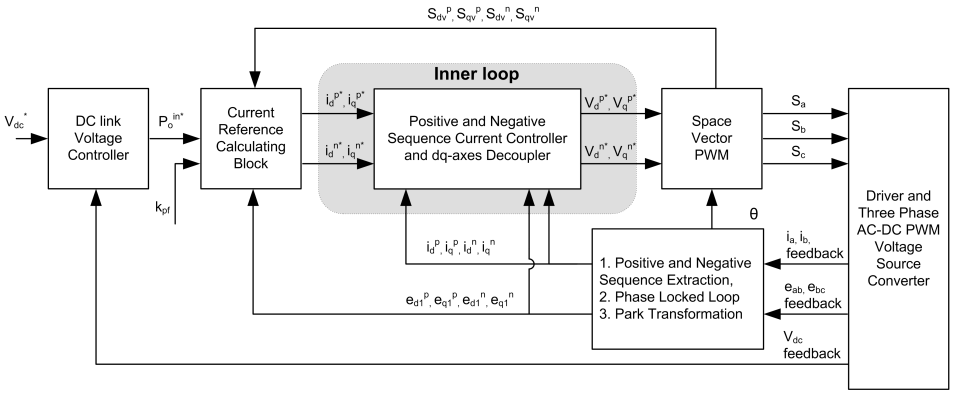

Fig. 2. Cascaded control block diagram of three phase PWM AC-DC boost rectifier

components. The *line side current harmonics control* is mainly to eliminate the 6th and 12th order harmonics in the line side currents represented in the *d-q* frame. For the periodic errors, repetitive control (RC) is a good choice for improving the tracking performance, i.e., to suppress the harmonic components of the certain frequency in the currents i_d^p, i_q^p, i_d^n and i_q^n by generating a compensation control signals S_d^p, S_q^p, S_d^n and S_q^n. The details of the repetitive controller scheme would be discussed in Section-4.

4. FREQUENCY DOMAIN BASED REPETITIVE CONTROLLER (FDRC) FOR THREE PHASE PWM RECTIFIER

Repetitive control is specially designed to remove the errors due to the fundamental and harmonics of the periodic inputs. Comparing to the commonly used TDRC, the learning algorithm of FDRC is implemented in the frequency domain by using Fourier series approximation (FSA) method. As a result, the knowledge of previous cycle error and control effort for each frequency can be utilized to eliminate periodic error in current cycle. The proposed current control scheme consists of the conventional PI controller together with a plug-in type frequency domain based repetitive controller for PWM rectifier as shown in Fig. 3.

The control output signal for the FDRC is given by,

$$u_{k+1} = FSA_u(u_k) + K_{rc} \cdot FSA_e(e_k) \cdot \tag{13}$$

where k is the cycle number; K_{rc} is a vector for the learning gain; u_{k+1} and u_k are the control inputs of the present and previous cycles respectively; e_k is the previous cycle tracking error; $FSA_e(e_k)$ and $FSA_u(u_k)$ are Fourier series approximation of previous cycle error and control signal respectively.

Fourier series approximation used for error signal e_k and control signal u_k can present a continuous periodic signal $f(t)$, which is defined over the time interval $0 \le t < T$ for one cycle and sampled with sampling time ΔT,

$$f(k\Delta T) = R_0 + \sum_{n=1}^{V-1} (R_n \cos(n\omega k\Delta T) + I_n \sin(n\omega k\Delta T)) \tag{14}$$

where

$$R_0 = \frac{\Delta T}{T} \sum_{k=0}^{N-1} f(k\Delta T) \tag{15}$$

$$R_n = \frac{2\Delta T}{T} \sum_{k=0}^{N-1} f(k\Delta T) \cos(n\omega k\Delta T) \tag{16}$$

$$I_n = \frac{2\Delta T}{T} \sum_{k=0}^{N-1} f(k\Delta T) \sin(n\omega k\Delta T) \tag{17}$$

where $n = 1, 2, 3, ..., V-1$; $k = 0, 1, 2, ..., N-1$; N denotes sampling number in the interval $0 \le t < T$; V is the number of harmonics; $\omega = 2\pi/T$.

The control objective of *line side current harmonics control* described in Section-3 is to eliminate 6th and 12th order harmonics in the positive and negative rotating synchronous *d-q* frame line currents. Therefore, the 300Hz, 600Hz frequency components are selected as the learning objectives and the learning gain are given for each component accordingly.

The FSA calculation algorithm employed in the controller can be simplified as the product of the frequency component vector and the coefficient vector. The frequency component vector of the tracking error is given as,

$$\Omega_e(k\Delta T) = \begin{bmatrix} 1 & \cos(6k\Delta T) & \cos(12k\Delta T) \\ & \sin(6k\Delta T) & \sin(12k\Delta T) \end{bmatrix} \tag{18}$$

Since the vector of the learning gain K_{rc} is $[\, K_6 \;\; K_{12} \,]$, the coefficient vector of the tracking error is given as,

$$\Psi_e(k\Delta T) = \begin{bmatrix} R_0 & K_6 R_6 & K_{12} R_{12} \\ & K_6 I_6 & K_{12} I_{12} \end{bmatrix}^T \tag{19}$$

In every sampling point, FDRC updates its coefficient vector $\Psi_e(k\Delta T)$ based on previous cycle information and calculates its frequency component vector $\Omega_e(k\Delta T)$. By using FSA, we can obtain,

$$FSA_e(f(k\Delta T)) = \Omega_e(k\Delta T) \times \Psi_e(k\Delta T) \tag{20}$$

The similar method can be used for the FSA of the control signals. However, the analog anti-aliasing filter shown in Fig. 3 and the plant characteristics introduce the phase delays between the output control signals and the feedback signals. Due to the presence of phase delay, the internal model of RC cannot be kept accurate. This phase delay problem which commonly exists in all control systems lead to the ineffective error minimization. Additionally, the

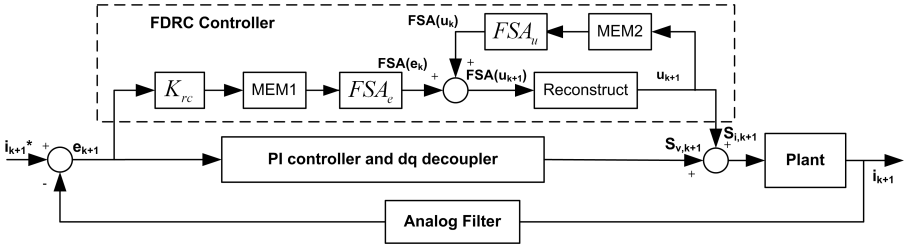

Fig. 3. Block diagram of PI controller with a plug-in type frequency domain based repetitive controller

phase delay for each frequency component is not the same and differ from one to another. Wu et al. [2007] shows that TDRC only can provide a fixed phase delay compensator for all the frequency components. Unlike in TDRC, FDRC can extract the magnitude and phase angle information for each frequency component separately and , the phase delay compensation could be easily added in to (18), so that Ω can be modified as,

$$\Omega_u(k\Delta T) = \begin{bmatrix} 1 & \cos(6k\Delta T + \alpha_6) & \cos(12k\Delta T + \alpha_{12}) \\ & \sin(6k\Delta T + \alpha_6) & \sin(12k\Delta T + \alpha_{12}) \end{bmatrix} \quad (21)$$

where α_6, α_{12} are the phase delays caused by the filter and the plant for the 6th and 12th harmonic components, respectively.

The FSA of the control signal can expressed as,

$$FSA_u(f(k\Delta T)) = \Omega_u(k\Delta T) \times \Psi_u(k\Delta T) \quad (22)$$

5. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed control scheme, the experiments were conducted under the unbalanced operating conditions. The complete control scheme was implemented on a dSPACE platform (DS1104). The DSP processor TI TMS320F240 was employed with 10 kHz sampling rate in the control board. The IGBT module adopted the symmetric PWM modulation with 20 kHz switching frequency. The frequency considered in Fourier series approximation for FDRC scheme are 300 Hz and 600 Hz. The computation time of this plug-in controller is around 30 μs. The detail system parameters used in the experimental platform are summarized in Table 1.

Table 1. Parameters Used In the Experiment

Parameters	Value	Parameters	Value
R	0.3 Ω	R_{dc}	225 Ω
L	0.005 H	C	200 μF
E_{rms}	80 V	$V_{dc,ref}$	400 V
K_{pc}	4	K_{ic}	250
K_{pv}	0.03	K_{iv}	4.59
K_6	1	K_{12}	2
α_6	0.75 rad	α_{12}	1.88 rad

Fig. 4 and Fig. 5 show the performance of the PWM rectifier without and with the proposed hybrid frequency domain based repetitive control scheme when 10% of the 5th order harmonic voltages are injected in the supply voltages. Without using FDRC, Fig. 4 shows the dc link voltage, phase-a ac line voltage and current of the system. The distorted supply voltages cause 5th and 7th order harmonics in the ac line currents to be 4.90% and 20.00%, respectively. The total harmonics distortion (THD) factor of the phase a input current is 21.09%. When the plug-in repetitive controller is activated, the current harmonics are reduced significantly as can be seen in Fig. 5. From the frequency spectra of the harmonics in the ac line currents, we can see that the 5th order harmonic component decreases from 4.95% to 0.57% and 7th order harmonics is from 20.00% to 0.96%, and the THD of the phase input current is reduced from 21.09% to 4.12%.

Fig. 6 and Fig. 7 show experimental results of the steady state current i_d^p in the positive rotating synchronous d-q frame and the frequency spectra of this current without and with the frequency domain based repetitive controller. Before using FDRC, there are obvious 6th (300Hz) and 12th (600Hz) order harmonics in the current i_d^p, which is caused by the distorted supply voltage. From Fig. 6, we can see that the amplitude of the 6th and 12th order harmonic components are 0.7891A and 0.1025A, respectively. Once FDRC is applied to eliminate the 300Hz and 600Hz frequency components, the harmonics in the current i_d^p has been significantly reduced as shown in Fig. 7. The magnitude of the 6th order harmonic component decreases from 0.789A to 0.04323A, and the 12th order harmonic component reduces from 0.1026A to 0.03119A.

Therefore, it can be concluded that the plug-in repetitive controller can minimize the harmonics in the supply side currents and provide better steady state performance under the distorted supply voltage operating conditions as compared to the conventional controller.

6. CONCLUSIONS

In this paper, a frequency domain based repetitive control scheme is proposed for the three phase PWM boost rectifiers to eliminate the supply side current harmonics under the generalized supply voltage conditions. The control task of the three phase PWM boost rectifier under the distorted and unbalanced supply voltage operating conditions can be divided into *voltage harmonics control* and *current harmonics control*. A plug-in frequency domain based repetitive current controller (FDRC), is employed as *current harmonics control* scheme by using Fourier series approximation (FSA) method. The learning algorithm of FDRC designed in frequency domain gives the freedom of choosing different learning gains and phase delay compensation individually for each harmonic component, which leads to the improved tracking performance for the ac line side currents. The experimental results verify that the THD of the line side current can be reduced from 21.09% to 4.12% with the insertion of the plug-in frequency domain based repetitive controller while maintaining the dc link voltage constant.

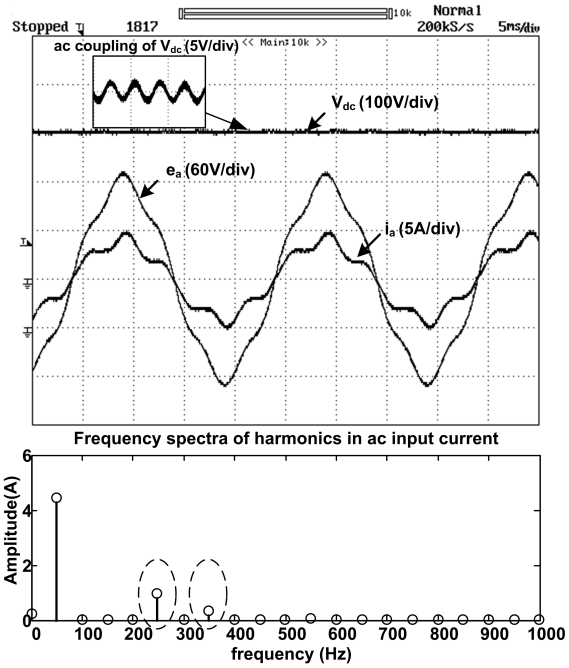

Fig. 4. Experiment results of dc link voltage and ac line current before using the repetitive controller

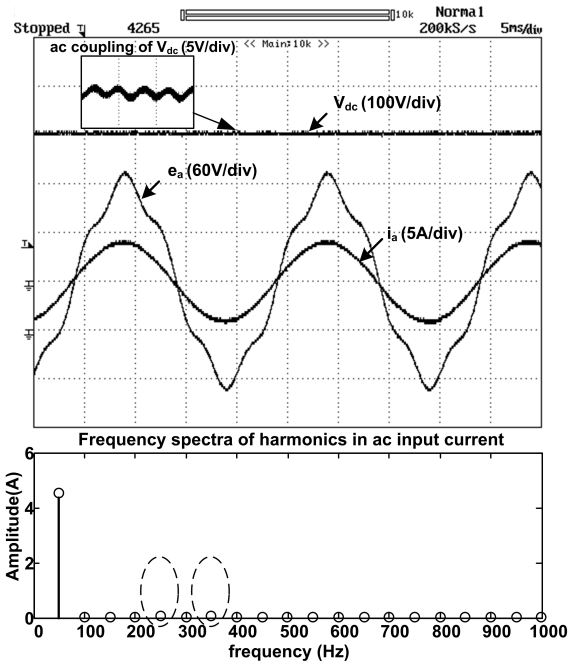

Fig. 5. Experiment results of dc link voltage and ac line current after using the repetitive controller

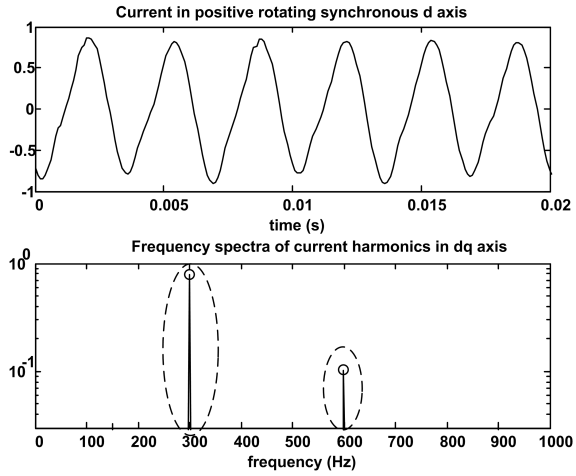

Fig. 6. Experimental results of the current i_d^p and its frequency spectra without using FDRC

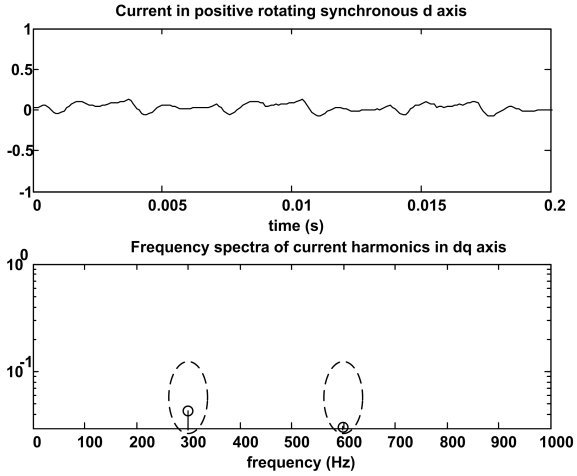

Fig. 7. Experimental results of the current i_d^p and its frequency spectra with using FDRC

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