Proceedings of the 17th World Congress
The International Federation of Automatic Control
Seoul, Korea, July 6-11, 2008

IFAC

Temperature Cycling for Photoresist Processing ⋆

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Abstract: A programmable multizone thermal processing module together with a model-based feedback control method are developed to achieve temperature uniformity of a silicon wafer throughout the processing temperature cycle of ramp, hold and quench in post-exposure bake (PEB) step of lithography. The module comprises of numerous small thermoelectric devices (TEDs) capable of precise substrate spatial temperature control. The detailed thermal modeling of the module is presented and the simulation results are compared with the experimental results to verify its feasibility. A model-based PID feedback control method is employed to minimize temperature nonuniformity across the wafer. With the method, temperature nonuniformity could be controlled less than 0.1°C throughout the entire thermal cycle. Advanced applications are enabled due to the proposed system.

1. INTRODUCTION

Chemically amplified resists (CARs) are employed in photolithography at wavelengths of 248 and 193 nm, for sub-100 nm pattern definition (ITRS [2006]). In such processes, the PEB step is becoming the major contributor of across wafer gate critical dimension (CD) variability. The variation in CD for this thermally activated process ranges generally between 1 to 10 nm/$°C$ in bake temperature (Parker, et al. [1997]). Recent investigations also show the importance of proper temperature uniformity, both during steady state and transient conditions, in significantly enhancing the CD uniformity across a wafer (Cain, et al. [2005], Goto, et al. [2006]). In conventional resist processing, the bake step is performed by placing the substrate on a fixed temperature bake plate and then mechanically transferring it to a fixed temperature chill plate. The plate is usually thermally massive and is maintained at a constant temperature by a feedback controller. Because of its large thermal mass and sluggish dynamics, conventional hotplates are robust to large temperature fluctuations and loading effects, and demonstrate good long-term stability. These advantages however become shortcomings in terms of process control and achievable performance when tight tolerances must be maintained. Other disadvantages include uncontrolled and non-uniform temperature fluctuation during the mechanical transfer of the substrates from the bake to chill plates, spatial temperature non-uniformities during the entire thermal cycle, etc (Schaper, et al. [1999]). This lack of a method to conduct real-time distributed, closed-loop temperature control with conventional hot plate is a source of process error in the lithography chain. Efforts in addressing some of these issues have been on-going by our collaborators and us (El-Awady, et al. [1999], Schaper, et al. [1999], Tay, et al. [2007]).

A fluid-heat-exchanger based thermal cycling module was earlier developed (El-Awady, et al. [1999]). The module provides thermal cycling by alternating between hot and cold fluids. The system has a much lower thermal mass than conventional units, but still requires large amounts of power for thermal cycling. A considerable improvement was achieved in a spatially programmable module using an array of cartridge heaters developed by Kailath's group in Stanford (Schaper, et al. [1999]) and subsequently commercialized. This system is excellent for processing substrates but without modification, it may not be able to achieve fast enough ramp-down rates during a thermal cycling operation. A notable exception is our recent work featuring a lamp thermoelectricity based integrated bake/chill system (Tay, et al. [2007])). The system consists of multiple radiant heating zones coupled with an array of thermoelectric devices (TEDs). We demonstrated that it satisfied tight spatial and temporal temperature uniformity specifications with a simple decentralized control scheme. However the lamp-based system consumes a lot of electrical power on account of the fact that a substantial amount of the radiant power is reflected from, and transmitted through, the wafer. In addition our present proposed system is physically more compact than the lamp-based counterpart and consequently better for implementation.

In this paper, we describe a programmable multizone thermal processing system and a model-based PID feedback

⋆ This work was supported in part by the Agency for Science, Technology and Research, Singapore under grant no. R263000426305.

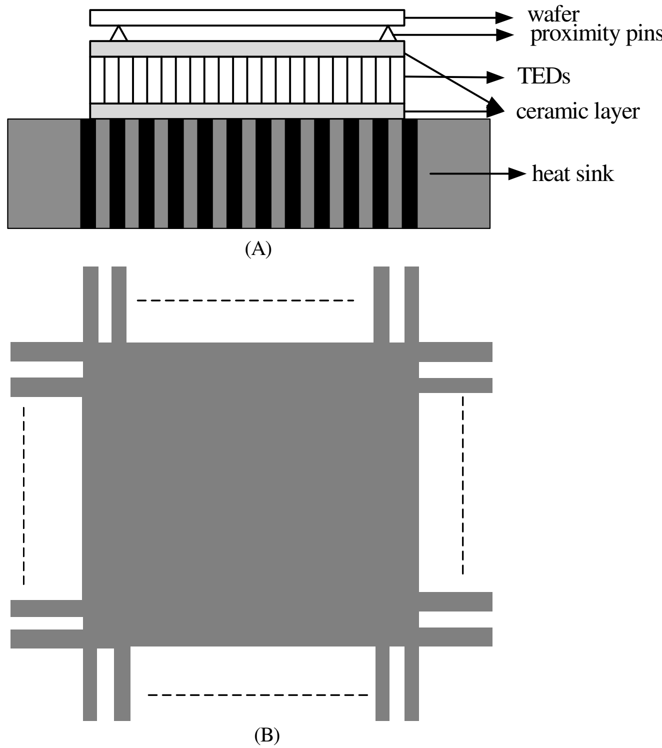

Fig. 1. Schematic diagram of the integrated bake/chill design. (A) schematic drawing of the system, (B) plan view of the heat sink. (Note: Figures are not drawn to scale)

control method for optimal processing of temperature sensitive photoresist to address the above mentioned issues. The design is based on detailed thermal modeling. In the proposed system, an array of TEDs is employed to provide spatial and temporal temperature uniformity control and active cooling so that we completely eliminate substrate movement and the attendant temperature uncontrollability between the baking and chilling processes. The temperature nonunifomity across the wafer is controlled to less than $0.1°C$ in experiment. The proposed system is also used in the processing of CARs, demonstrating uniform linewidth control compared to conventional approaches.

2. THERMAL MODELING OF THE PROPOSED THERMAL PROCESSING SYSTEM

A schematic of the proposed thermal processing module is shown in Fig. 1 (A). In the system, wafer sits on an array of proximity pins and spaces approximately 5 mils above the bismuth telluride TEDs. These proximity pins can be embedded with temperature sensors (Minco [2006]) to provide in-situ temperature measurement. The TEDs rest on top of a heat sink and integrally form the cooling mechanism. (B) shows the top view of the heat sink. We will next consider the governing thermal equations for the essential components in the system.

2.1 Heat Transfer in Wafer

A typical wafer thickness is 0.675mm. This is sufficiently thin to consider a uniform temperature across the thickness of the wafer. Considering both heat conduction and

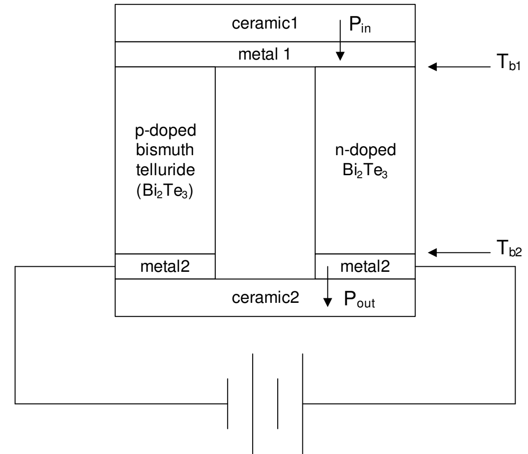

Fig. 2. Schematic diagram of a thermoelectric element. (Note: Figure is not drawn to scale)

convection, we invoke a two-dimensional transient heat diffusion equation and adopt a finite-difference numerical technique. For each wafer element, we have

$$\rho v_{i,j} c_p \frac{\partial T}{\partial t} = q_{i,j}^{up} + q_{i,j}^{down} + q_{i,j}^{left} + q_{i,j}^{right} + q_{i,j}^{top} + q_{i,j}^{bottom} + q_{i,j}^{conv} \tag{1}$$

where T is the temperature, ρ the density, v the volume c_p the heat capacity and $q_{i,j}^{up}, q_{i,j}^{down}, q_{i,j}^{left}, q_{i,j}^{right}, q_{i,j}^{top}$ and $q_{i,j}^{bottom}$ are respectively the heat flow rate into the (i,j) wafer element from the $(i,j+1),(i,j-1),(i-1,j),(i+1,j)$ element, air on top and below the (i,j) element. $q_{i,j}^{conv}$ is relevant to elements at the edge of the wafer and refers to the heat flow rate into the element from the side surface via convection.

The wafer's top surface is exposed to the surroundings and so we have

$$q_{i,j}^{top} = hA_{i,j}^{top}(T_{ambient} - T_{w(i,j)}) \tag{2}$$

where h the heat convection coefficient and the subscript *ambient* denotes the ambient air.

The air gap between the wafer and TEDs is 5 mils. Since it is much less than$5.8mm$, and their temperature difference is considerably smaller than $200°C$ (Hollands, et al. [1975]), the heat transfer mechanism is essentially conductive and given by

$$q^{bottom} = -k_{ag}A_{ag}\frac{\partial T_{ag}}{\partial z_{ag}}|_{boundary} \tag{3}$$

where A is the cross-sectional area and the subscribe ag denotes the air gap.

The convective heat transfer between each element (i,j) of wafer and surrounding air is given by

$$q_{i,j}^{conv} = hAs_{(i,j)}(T_{ambient} - T_{w(i,j)}) \tag{4}$$

where $A_{s(i,j)}$ is the side surface area of the edge element.

2.2 Thermoelectric Devices (TEDs) Modeling

A thermoelectric device is composed of different layers of material with different properties, including ceramic layers, metal films and thermoelectric elements as shown in Fig. 2. The metal film is sandwiched between thermo-

electric elements and the ceramic substrates. The Peltier Seebeck, Thomson and Joulean effects are the governing principles of thermoelectricity. For bismuth telluride, the Thomson effect is insignificant so it is neglected in the simulation (Chua, et al. [2002]). Consequently, the governing thermal transport in the semiconductor arms is given by (Rowe [1994])

$$\rho_t c_{p,t} \frac{\partial T_t}{\partial t} = k_t \frac{\partial^2 T_t}{\partial z_t^2} + \frac{J^2}{\sigma_t} \quad (5)$$

where σ is the electrical conductivity, $J(= I/A)$ the current flux where I and A are respectively the direct current flowing through the TEDs and the cross-sectional area. The subscript t denotes the thermoelectric modules.

The Peltier effect is manifested at the boundary between the TED's metal contacts and the thermoelectric elements. It is given by:

$$k_t A_t \frac{\partial T_t}{\partial z_t} + k_m A_m \frac{\partial T_m}{\partial z_m} \pm \alpha I T_{bd} = 0 \quad (6)$$

where α is the Seebeck coefficient and the subscripts m and bd denotes the metal film contacts in the TEDs and the boundary layer respectively. The first two temperature gradient terms denote the temperature gradient from the boundary to the corresponding materials. The last term denotes the Peltier effect at the boundary. The sign in the last term in equation (6) is positive in heating mode and negative in chilling mode. The thermal transport phenomenon in the metal film element is similarly expressed as

$$\rho_m c_{p,m} \frac{\partial T_m}{\partial t} = k_m \frac{\partial^2 T_m}{\partial z_m^2} + \frac{J^2}{\sigma_m} \quad (7)$$

The governing thermal transport equation of the ceramic substrate is

$$\rho_{ce} c_{p,ce} \frac{\partial T_{ce}}{\partial t} = k_{ce} \frac{\partial^2 T_{ce}}{\partial z_{ce}^2} \quad (8)$$

where the subscripts ce denotes the ceramic substrate.

The boundary heat transfer equation at the interfaces between ceramic and metallization of a TED is expressed below as a mixed boundary condition:

$$-k_a A_a \frac{\partial T_a}{\partial z_a}|_{boundary} = -k_b A_b \frac{\partial T_b}{\partial z_b}|_{boundary} \quad (9)$$

The electricity power consumed by each TED zone can be computed via an energy balance as

$$P_{electricity} = [P_{out} - P_{in} + \triangle P + 2\alpha I(T_{b1} - T_{b2})]N \quad (10)$$

where $P_{out} = -k_m A_m \frac{\partial T_{m2}}{\partial z_{m2}}$, is the energy transferred from metal2 to ceramic2; $P_{in} = -k_{ce} A_{ce} \frac{\partial T_{ce1}}{\partial z_{ce1}}$, the energy transferred from ceramic1 to metal1; $\triangle P = \sum_i \int_{vi} \rho_i c_{p,i} \frac{\partial T_i}{\partial t} dv_i$, the rate of change of internal energy, i stands for metal1, metal2 or TED; N is the number of pairs of TED arms in a particular zone and T_{b1}, T_{b2} are the respective metal-ceramic boundary temperatures.

2.3 Heat Sink Modeling

During the cooling process, heat absorbed at the cold junction of TEDs is pumped to the hot junction at a rate proportional to the current passing through the circuit.

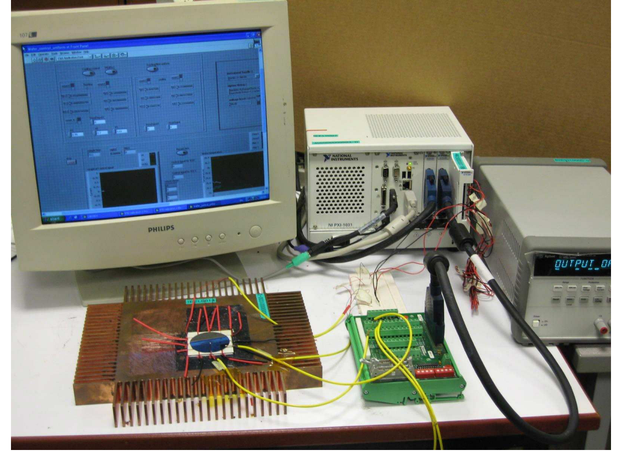

Fig. 3. Photograph of the experimental setup.

At the hot junction, the absorbed energy needs to be dissipated via a heat dissipating device. To meet this target, a heat sink with extended fins is designed. On account of the thermal conductivity of copper in relation to the convective heat transfer coefficients, we assign the heat sink with a uniform temperature. The governing thermal equation of the heat sink is accordingly expressed as

$$\rho_{hs} c_{p,hs} \frac{\partial T_{hs}}{\partial t} = k_{ce} A_{ce} \frac{T_{ce} - T_{hs}}{Z_{ce}/2} + (\eta_0 h_{a,f} A_{a,f} + h_{a,s} A_{a,s})(T_{ambient} - T_{hs}) \quad (11)$$

where η_0 is the fin efficiency of the heat sink and the subscript hs denotes heat sink.

Designing for a heat sink equilibrium temperature, we require the convection heat transfer coefficient of the designed heat sink to satisfy

$$t_{cd}(P_w + P_{mi} + P_{electricity}) \leq t_{cc} \times (\eta_0 h_{a,f} A_{a,f} + h_{a,s} A_{a,s})(T_{hs,E} - T_{ambient}) \quad (12)$$

where t_{cd} is the time needed to cool wafer from 100°C to room temperature and t_{cc} is the time period of the cooling cycle. With the inequality, we designed a heat sink as shown in Fig. 1(B). Simulations show that the designed heat sink would equilibrate at $T_{hs,E} \approx 57.5°C$ after several consecutive thermal cycles. So the heat sink can dissipate heat effectively and will stabilize at the intended temperature.

3. EXPERIMENTAL SETUP

Based on the thermal modeling analysis and simulations in section 2, a prototype system is developed for the control of 2-inch silicon wafer. A photograph of the 2-zone prototype thermal processing system is shown in Fig. 3. Two RTD sensors are positioned on the 2-inch wafer to monitor the temperature of the two zones. The TEDs are discretized into 2 pseudo-circular zones and dictated by the calculated control signal to provide desired heating and cooling process and maintain temperature uniformity. In each zone, the elements are all excited similarly and one temperature sensor is chosen to represents its temperature. The temperature distribution within each zone is assumed at any instant to be sufficiently uniform that the temperature of the zone can be considered to be a function of time only.

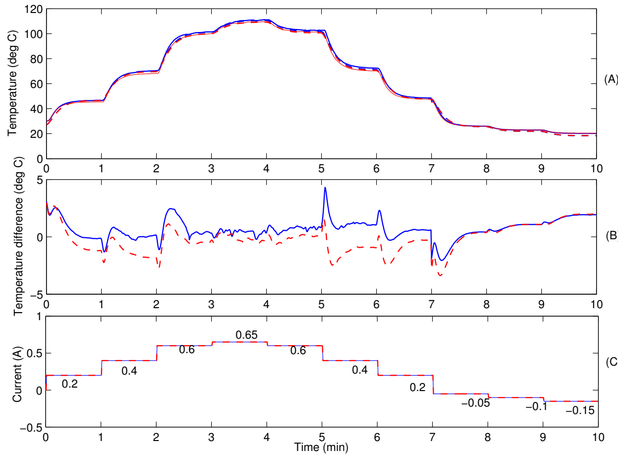

Fig. 4. Comparison of experimental and simulation wafer temperature using different input signals. (A) wafer temperature responses, the solid line shows the zone1 and zone2 wafer temperature in experiment and the dashed line shows the zone1 and zone2 wafer temperature in simulation, (B) wafer temperature difference between experiment and simulation, the solid line shows the temperature difference of zone1 and the dashed line shows the temperature difference of zone2, (C) input current in the process.

To estimate the performance of simulation model, different input currents are injected into the system, and the comparison of the experimental and simulation result is shown in Fig. 4.

In the experiment, the input signal is chosen to be 0.2A, 0.4A, 0.6A, 0.65A, 0.6A, 0.4A, 0.2A, -0.05A, -0.1A, and -0.15A respectively and each hold for 1 minute. Fig. 4 (A) shows the wafer temperature in experiment and simulation where the solid line shows the zone1 and zone2 wafer temperature in experiment and the dashed line shows the zone1 and zone2 wafer temperature in simulation. Fig. 4 (B) shows the temperature difference between experiment and simulation and Fig. 4 (C) features the input current in the process. It can be seen that the simulation and experimental wafer temperature can match very well with different input signals, which verify the effectiveness of the thermal modeling.

The comparison of the experimental and simulation result of the 5 consecutive cycles is shown in Fig. 5. Fig. 5 (A) shows the wafer temperature in experiment and simulation. Fig. 5 (B) shows the temperature difference between experiment and simulation. It can be seen that the simulation and experimental wafer temperature can fit well in the process and the system can still work well after several consecutive runs. This verifies the feasibility of the proposed system with the designed heat sink.

The heat sink temperature in the simulation and experiment is shown in Fig. 6. Fig. 6 (A) shows the heat sink temperature in experiment and simulation and Fig. 6 (B) shows the temperature difference between experiment and simulation. We can see that the experimental heat sink temperature is very close to the simulation temperature. We note that the heat sink temperature continues to rise as it has not reach its steady-state equilibrium condition.

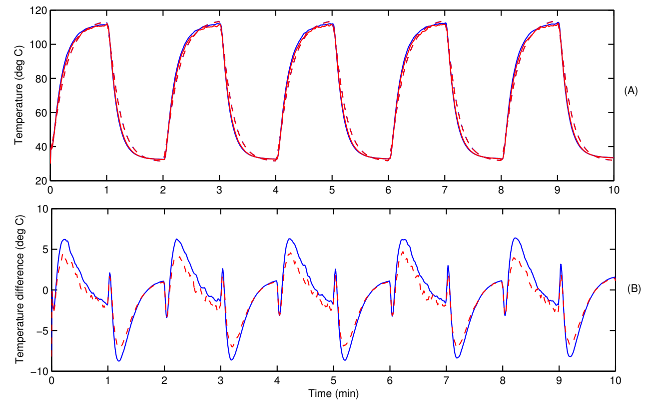

Fig. 5. Comparison of experimental and simulation wafer temperature in 5 consecutive cycles. (A) wafer temperature responses, the solid line shows the zone1 and zone2 wafer temperature in experiment and the dashed line shows the zone1 and zone2 wafer temperature in simulation, (B) wafer temperature difference between experiment and simulation, the solid line shows the temperature difference of zone1 and the dashed line shows the temperature difference of zone2.

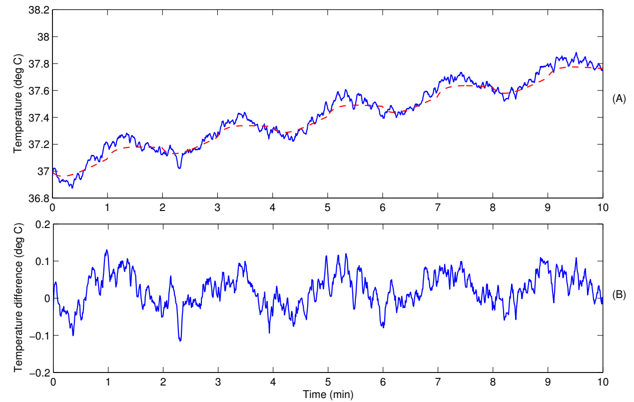

Fig. 6. Comparison of experimental and simulation heat sink temperature in 5 consecutive cycles. (A) heat sink temperature responses, the solid line shows the heat sink temperature in experiment and the dashed line shows the heat sink temperature in simulation, (B) temperature difference between experiment and simulation.

4. MODEL-BASED CONTROLLER

4.1 Model-based Controller Design

Two objectives are sought in a closed-loop controller. The controller should provide the necessary transient and steady-state uniformity, as well as following the system set point. Consider the plant described by transfer function matrix

$$\begin{bmatrix} T_{w1} \\ T_{w2} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \end{bmatrix} \tag{13}$$

where T_{w1} and T_{w2} represent temperature change of wafer's zone1 and zone2 respectively, and P_1 and P_2 represent the current change in TEDs of zone1 and zone2 respectively. To guarantee the temperature uniformity of the two zones we need

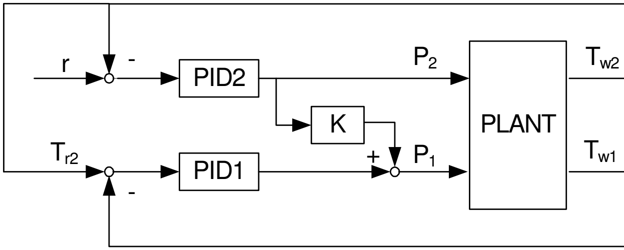

Fig. 7. Block diagram of the proposed model-based control scheme.

$$T_{w1} = T_{w2} \tag{14}$$

With the model of the system, this equation can be expressed as

$$G_{11}P_1 + G_{12}P_2 = G_{21}P_1 + G_{22}P_2 \tag{15}$$

Then, we can get the ratio of the two zones control signal:

$$K = \frac{P_1}{P_2} = \frac{G_{22} - G_{12}}{G_{11} - G_{21}} \tag{16}$$

P_2 is used to track the set point, while $P_1 = KP_2$ is used to minimize the temperature difference between the two zones. The approach can be easily extended to an n-zone system. The block diagram the control strategy is shown in Fig. 7.

4.2 System Identification

Prior to implementing the control scheme on the thermal processing system, a model for the system must first be identified experimentally. The model relates the change in wafer temperature to the change in TEDs' current. It is determined by injecting two independent pseudo random binary sequences (PRBS) (Landau [1990]) into the TEDs' two control zones respectively as shown in Fig. 8. Using least squares estimation, the process model is identified as

$$\begin{aligned} G_{11} &= \frac{1.482q^{-3}}{1 - 0.9681q^{-1}} \quad G_{12} = \frac{0.956q^{-4}}{1 - 0.9796q^{-1}} \\ G_{21} &= \frac{0.524q^{-6}}{1 - 0.9625q^{-1}} \quad G_{22} = \frac{1.101q^{-3}}{1 - 0.9767q^{-1}} \end{aligned} \tag{17}$$

With the identified model, the ratio K can be calculated as

$$K = \frac{G_{22} - G_{12}}{G_{11} - G_{21}} = \frac{1.101 - 2.034q^{-1} + 0.934q^{-2}}{1.482 - 1.4301q^{-1} - 0.524q^{-3} + 0.507q^{-4}}$$

$$\times \frac{1 - 1.9306q^{-1} + 0.9318q^{-2}}{1 - 1.9563q^{-1} + 0.9568q^{-2}} \tag{18}$$

5. EXPERIMENTAL RESULTS

Fig. 9 shows the temperature uniformity during a typical thermal cycle. The top plot shows the wafer temperature in baking process. The middle plot shows the temperature nonuniformity of the wafer. The bottom plot shows the control input. It can be seen that the TEDs current input is positive in baking process to provide heating effect to the wafer and is negative in cooling process to provide chilling effect to the wafer. The wafer can be heated to desired temperature and chilled to room temperature with the

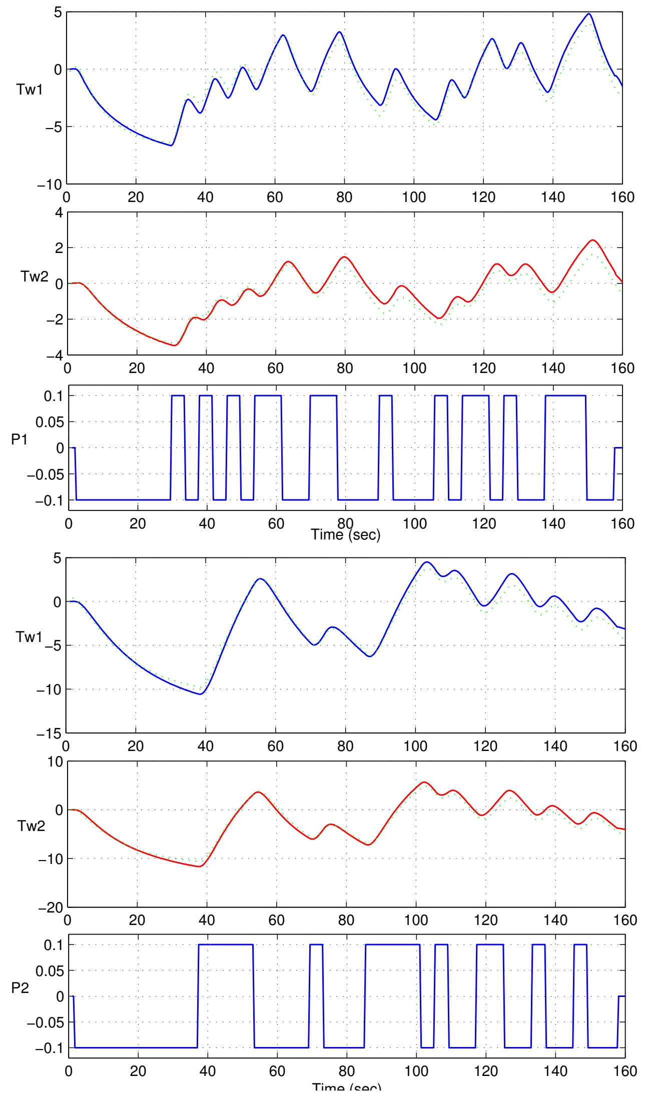

Fig. 8. System identification result with two independent pseudo-binary random sequences injected into two control zones respectively. The solid line shows the resulting change in wafer temperature and the dotted line shows the calculated response using the identified model.

single processing system and during the whole process the temperature nonuniformity can be maintained less than $0.1°C$ as desired.

5.1 Real-time CD uniformity control

We next demonstrate the capability of the programmable multizone thermal system. The linewidth of critical dimension (CD) is the most critical parameter in the manufacturing of integrated circuits. Variation in CD control results in scrapped product due to slow processing speeds or high leakage rates. For current generation of photoresist, the temperature of the wafer during this thermal cycle has to be controlled to a high degree of precision both spatially and temporally. A number of recent investigations also show the importance of proper bakeplate operation on CD control Friedberg, et al. [2004]. The ability to control the temperature of the wafer to different setpoint is exploited in this application.

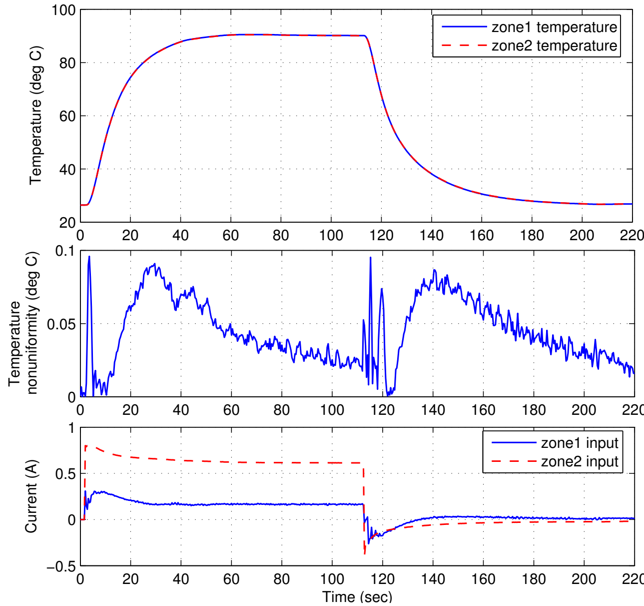

Fig. 9. Experimental result of the bake/chill integrated system using the model-based control method.

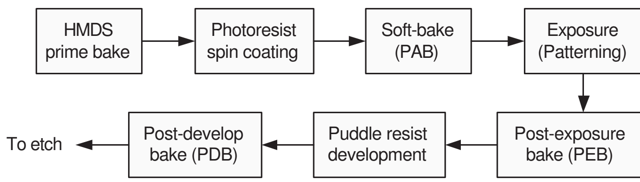

Fig. 10. The lithography sequence.

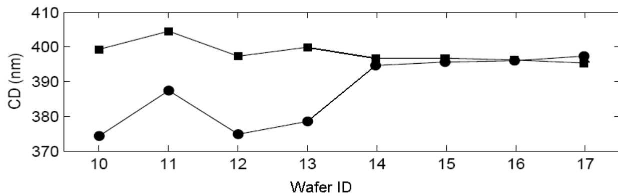

Fig. 11. Real-time CD uniformity control. Circle is the center of wafer and square indicate the edge of the wafer.

Fig. 10 shows the various baking operations in the lithography sequence. In our application, we control the CD uniformity using the softbake process. After the spin-coating process, the coated resist is usually non-uniform, the subsequent bake step is then used to manipulate the wafer temperature such that higher temperature heating is induced at location where the resist is thicker. This is easily achieved with our programmable multizone system, where an array of thickness sensor can be mounted above the wafer to monitor the thickness in real-time. In all our experiments, commercial chemical amplified resist, Shipley UV3 was spin-coated on the wafer. Fig. 11 shows the CD uniformity at the center and edge of the wafer before and after the multizone system is employed. The CD non-uniformity has improved from about 20nm to 1nm.

6. CONCLUSION

An integrated bake/chill module for photoresist processing in lithography is presented, rigorously simulated and experimentally demonstrated. The detailed thermal modeling of the system is analyzed based on first principle heat transfer. Based on the model, simulations are carried out to verify the feasibility of the system. The distributed nature of the design also engenders a simple decentralized control scheme which satisfies tight spatial and temporal temperature uniformity specifications. Transient and steady-state temperature uniformity of less than 0.1^{o}C can be achieved. Advanced application such as real-time CD control is also demonstrated.

REFERENCES

J. Cain, P. Naulleau, and C. Spanos. Critical dimension sensitivity to post-exposure bake temperature variations in EUV photoresists. *Proceedings of the SPIE*, volume 5751, pages 1092-1100, 2005.

H.T. Chua, K.C. Ng, X.C. Xuan, C. Yap, and J.M. Gordon. Temperature entropy formulation of thermoelectric thermodynamic cycles. *Physics Review E*, volume 65, 2002.

K. El-Awady, C.D. Schaper, and T. Kailath. Integrated Bake/chill for Photoresist Processing *IEEE Trans. Semiconductor Manufactering*, volume 12, no 2, pages 264-266, 1999.

S. Goto, K. Matsuchika, and A. Hisai. Integrated Bake/chill for Photoresist Processing. *Proceedings of the SPIE*, volume 6153, 2005.

K. G. Hollands, G.Raithby, and L. Konicek. Correlation equations for free convection heat transfer in horizontal layers of air and water. *International Journal of Heat Mass transfer*, volume 18, pages 879, 1975.

International Technology Roadmap for Semiconductors, 2006 updated version.

I.D. Landau. *System Identification and Control Design.* Prentice Hall, 1990.

Minco Corporation, Thin film RTD elements, www.minco.com (2006).

J. Parker and W. Renken. Temperature metrology for CD control in DUV lithograpghy. *Semiconductor International*, volume 20, no 20, pages 111–116, 1997.

D.M. Rowe. *Handbook of Thermoelectrics*, CPC Press, New York, 1994.

C.D. Schaper, K. El-Awady, A. Tay, and T. Kailath. Control systems for the nanolithography process. *Proceedings of 38th IEEE Conference on Decision and Control*, volume 4 1999.

C.D. Schaper, K. El-Awady, and A. Tay. Spatially Programmable Temperature Control and Measurement for Chemically Amplified Photoresist Processing *Proceedings of SPIE*, volume 3882, pages 74-79, 1999.

A. Tay, H.T. Chua, X.D. Wu A lamp thermoelectricity based integrated bake/chill system for photoresist processing *International Journal of Heat Mass Transfer*, volume 50, no 3-4, pages 580-594, 2007.

P. Friedberg, C. Tang, B. Singh, T. Brueckner, W. Gruendke, B. Schulz, C. Spanos, Time-based PEB adjustment for optimizing CD distributions, Proceeding of SPIE 5375(2004) 703-712.