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The Fault-tolerant Extension of System Area Networks of Multiprocessor System

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Abstract: The method is proposed for building a fault-tolerant system area network (SAN) as a flat network comprised of several copies of the source network. This flat network is based on a theory of balanced incomplete block designs (BIBD).

Key words: multiprocessor parallel computers, system area networks, fault-tolerant networks, balanced incomplete block designs.

1. INTRODUCTION

At present the multiprocessor system communication nets are widely known as *System Area Networks* (SAN), so we use this term in what follows. Initially, it is anticipated that system area networks (SAN) are fully accessible.

The problem of realizing *k*-fault-tolerant multiprocessor systems (MPS) with a minimum of redundant processors was stated in (Karavay 1996). In that problem statement it was suggested that there exists a working set of processors

$$W : |W| = N ,$$

and a set of hot standby ones

$$B : |B| = k .$$

Once any $t \le k$ processors from W have failed, the MPS reconfiguration is performed, to form a new W content by including in it any t processors from B. This reconfiguration is to be performed only by a replacement of address tables interpreted at a circuit level, without a retranslation of all applications running at a working processor set. Application execution times for any working processor set are to be equal at a prescribed accuracy.

This problem is solved in (Karavay 1996, 2000, 2004, 2005) under the assumption that MPS structure is defined by a point graph, while the application logical structure represented by a target graph along with relations between resources (target graph vertexes and arcs) and a schedule of their use is considered as an invariant of a fault-tolerant system. The method of solving this problem is based on a symmetrization of connections with respect to Hamilton circuits in a SAN.

The practicality of this method is restricted by the following factors: firstly, its complexity increases with increasing k; secondly, the fault-tolerance of SAN itself is assumed; thirdly, it is inapplicable in a case of SAN without Hamilton circuits, as in multistage switches.

The present work deals with a problem of imparting fault-tolerance to any SAN under the following assumptions. In the first place, a SAN may be isolated in the uncombined state being defined as a black box with an arbitrary structure of internal connections, where points of duplex connection of multiple processors are indicated. Second, the possibility exists of using several copies of SAN with different processor sets and of copy reduction. All copies are reduced in the same manner by eliminating some connection points. Thirdly, each processor may be connected to the same number of distinct copies of SAN.

SAN fault-tolerance is available by establishing multiple paths between any pair of processors through different copies of SAN. The fault-tolerance feature is provided by a minimum of distinct paths over all pairs of processors.

Here, a fault-tolerant SAN is constructed as a flat network comprised of multiple copies of the source SAN. Within such network any path between a pair of processors passes successively through a single copy of SAN only. The construction of flat SANs is based on a combinatorial theory (Hall 1961) of balanced incomplete block designs (BIBD). The mathematical theory of BIBD was derived in the mid-twentieth century for planning complete designs in areas of selection, genetics, and others. In the frame of this work it finds a new application.

The flat network construction was already considered in (Podlazov et al 2006a, b, 2007) as related to a delay-invariant extension of SAN, but the extended SANs investigated within

abovementioned publications were devoid of a fault-tolerance feature.
The present work combines a fault-tolerant SAN construction with its extension in a controllable scope. As this takes place, increasing processors in number may be treated also as addition of hot standby processors. Thus the construction of extended fault-tolerant SAN may serve a basis of a fault-tolerant MPS buildup.

2. BLOCK DESIGNS AND PRIMARY FLAT NETWORKS

Balanced block design $B(M, N, k, m, \sigma)$ is a set of M blocks, where N distinct elements occur in all blocks so that exactly k distinct elements occur in each block; each element occurs in exactly m blocks, and each pair of elements occurs in exactly σ blocks. On this block design definition, its parameters are related by the following equations:

$$Nm = kM\ ,$$
$$m(k-1) = \sigma(N-1), \quad k < N\ . \tag{1}$$

Block design definition with the accuracy to a transposition of elements in blocks and/or of blocks themselves is noteworthy. This being so, block designs distinguished by an order of element occurrence within blocks and/or by blocks ordering are equivalent to each other.

The mathematical theory of block designs is constructed for a case of $k \le m$, $N \le M$, when a block width is not in excess of the occurrence factor, and elements are not superior to blocks in number.

The minimum block count and maximum element count is provided in a case of symmetrical designs when $k = m$ and $M = N$. It is preciously these block designs $\hat{B}(N, m, \sigma)$ that are considered below. They have as few as three parameters: element occurrence factor m, element count $N = m(m-1)/\sigma+1$ and pair of elements occurrence ratio σ. Necessary conditions for existence of a symmetrical block design are defined (Hall 1961) by the BRC (Bruck, Ryser, Chowla) Theorem.
If there exists a symmetrical block design $\hat{B}(N, m, \sigma)$, then on putting $\eta = m - \sigma$ we obtain:
1) At even-numbered N parameter η is a square of an integral number;
2) At odd-numbered N the equation

$$z^2 = \eta x^2 + (-1)^{\frac{N-1}{2}} \sigma y^2$$

possesses a solution in integral numbers x, y, z, which are never all zero together.

It should be noted that the BRC Theorem presets very strong necessary conditions for the existence of symmetrical block designs, since the counterexamples remain unknown. Essentially these existence conditions may be thought of as sufficient ones also.

Now replace a block in a definition of the block design $\hat{B}(N, m, \sigma)$ by a copy of some source SAN, replace element by a SAN subscriber (processor, computer), replace element occurrence into a block design by a duplex connection of the subscriber to one of SAN copies, and lastly replace the block design by an extended SAN.
Denote a SAN of N subscribers by SAN(N). Now we can give a definition of an extended SAN. A fully accessible SAN(N) is proved to be the extended SAN, if it comprises of N copies of the source SAN(k), k different subscribers are connected to each copy, each subscriber is connected to m distinct copies of the source SAN(k), and there are σ parallel paths through distinct copies of the source SAN(k).

From the definition it follows that such additional circuit component as input/output (I/O) splitter/coupler $1\times m$ is required for connecting any subscriber to multiple copies of the source SAN to construct the extended SAN. As a result, the occurrence factor m becomes a factor of subscriber's I/O splitter/coupler, where delays fall far short of ones in the source SAN.

Under the present tendency to using a sequential point-to-point communication for interprocessor connections the said I/O splitter/couplers are embedded already into a chipset in the form of switching matrixes and extenders 1×2^n, as for instance, in *PCI-Express.*

From the definition it follows also that the extended SAN(N) is proved to be a flat SAN, since its any two subscribers are connected to one another sequentially through a single copy of the source SAN(k), saving in extended SAN such basic functional features of the source SAN as a routing possibility and, to a high accuracy, its communication delays.

Abovementioned extended SANs are isomorphic to block designs. Let us term them as primary flat networks (PFN) and denote them as PFN(N, m, σ). Table 1 gives a simple example of PFN with σ parallel paths, where $\sigma>1$. The first column defines the number of a source SAN copy; rows describe corresponding copies of the source SAN, and any cell indicates a number of subscriber coupled to a given copy. The described PFN is isomorphic to a cyclic block design (Hall 1961).

Table 1. PFN(7, 4, 2) with $\Sigma=(0, 1, 2, 4)$.

Copies of the source SAN	PFN(7, 4, 2)			
0	0	6	5	3
1	1	0	6	4
2	2	1	0	5
3	3	2	1	6
4	4	3	2	0
5	5	4	3	1
6	6	5	4	2

A cyclic PFN is represented by a table in which columns contain circularly shifted sequences 0, 1, …, N–1. These PFN will be defined by a set of numbers indicating that source SAN copies, to which a zero subscriber is coupled. Denote this set as Σ.

It should be noted that PFN does not exist for arbitrary Σ. The authors of this work implemented an exhaustive search algorithm (Σ-algorithm) for testing all possible Σ values to extract only those defining PFN. This Σ-algorithm searches $C_{N-1}^{m-1} = \binom{N-1}{m-1}$ values of Σ. If it is remembered that

$$\lim_{N\to\infty} N/m^2 = \sigma^{-1},$$

then we can write:

$$\lim_{N\to\infty} \frac{C_{N-1}^{m-1}}{\sigma^2 e^m m^{m-1,5}} = 1/\sqrt{2\pi}\ .$$

Therefore, for large values of N the Σ-algorithm has the complexity estimate $O(e^m m^{m-1,5})$, that is, becomes *NP*-complete by m.

Table 2. Parameters of PFNs that are allowable by formulae (1), and their attributes A: admissible (+), inadmissible (–), cyclic (#), non-cyclic ($), considered in (Hall 1961) (*), constructed using Σ-algorithm (!).

σ	1		2		3		4		5	
m	*N*	*A*	*N*	*A*	*N*	*A*	*N*	*A*	*N*	*A*
2	**3**	+#*!	**2**	+#*!						
3	**7**	+#*!	**4**	+#*!	**3**	+#*!				
4	13	+#*!	**7**	+#*!	**5**	+#*!	**4**	+#*!		
5	21	+#*!	**11**	+#*!			**6**	+#*!	**5**	+#*!
6	31	+#*!	16	+$*	**11**	+#!			**7**	+#*!
7	43	–*	22	–	**15**	+#*!				
8	57	+#*!	29	–			**15**	+#!		
9	73	+#*!	37	+#*!	25	+$*	**19**	+#*!		
10	91	+#*!	46	–	31	+$*			**19**	+#!
11	111	+$	56	+					**23**	+#*!
12	133	+#*	67	–	45	+$	34	–		
13	157	+$	79	+	53	–	40	+#!		
14	183	+#*	92	–						
15	211	–*	106	–	71	+			43	+
16	241	+$	121	+	81	+	61	+	49	+
17	273	+#	137	–			69	+		
18	307	+#	154	+	103	–				
19	343	+$	172	–	115	+				
20	381	+#	191	+			96	+	77	–
21	421	–	211	+	141	–	106	–	85	+

Cyclic PFNs are far from defining all possible PFN, which are described by formulae (1) and are allowable by the BRC Theorem. Table 2 shows all possible PFN obtained using formulae (1) for $m \le 21$. The plus sign (+) indicates admissibility in BRC Theorem; the minus sign (–) denotes inadmissibility. The symbol # marks a cyclic PFN; symbol $ denotes a non-cyclic PFN; asterisk character (*) indicates PFN, which are defined by a reference table from (Hall 1961), and exclamation mark (!) points PFNs constructed using Σ-algorithm.

Note that developing techniques for constructing even individual non-cyclic block designs $\hat{B}(N, m, \sigma)$ is a challenging research problem up till now. It will suffice to mention a problem of constructing a block design $\hat{B}(111, 11, 1)$, which came to be already a classical one. To buildup this block design, it is necessary to have 11 Greco-Latin squares of 10th order with distinct rows. Not all of them are found yet.

Note two paired diagonals in a Table 2 set off in a bold print. The PFNs outlined in these diagonals exist for any m=σ; by the BRC Theorem, they exist also for any m=σ+1 and m=2σ, m=2σ+1 at arbitrary σ≥1. They contain, accordingly, N=σ, N=σ+2, N=4σ–1 and N=4σ+3 copies of the source SAN for m subscribers, and unite N subscribers.

Table 2 (continued). Parameters of PFNs that are allowable by formulae (1) , and their attributes A: admissible (+), inadmissible (–), cyclic (#), non-cyclic ($), considered in (Hall 1961) (*), constructed using Σ-algorithm (!).

σ	6		7		8		9		10	
m	*N*	*A*	*N*	*A*	*N*	*A*	*N*	*A*	*N*	*A*
6	**6**	+#!								
7	**8**	+#*!	**7**	+#*!						
8			**9**	+#*!	**8**	+#*!				
9	13	+#!			**10**	+#*!	**9**	+#*!		
10	16	+$					**11**	+#*!	**10**	+#*!
11									**12**	+#*!
12	**23**	+#!								
13	**27**	+$*								
14			**27**	+$						
15	36	+$	**31**	+#*!						
16	41	+			**31**	+#!			25	+$
17					**35**	+#!				
18	52	–					**35**	#!		
19	58	–					**39**	+$		
20									**39**	+$
21	71	+	61	–					**43**	+#!

Definition 1. A flat SAN is proved to be l-fault-tolerant by links (that is, has the fault-tolerance factor l), if between any pair of subscribers there exist at least l+1 paths through distinct source SAN copies.

Now the following evident assertion.

Assertion 1. Any allowable PFN(N, m, σ) is (σ-1)-fault-tolerant by links.

Unfortunately, PFN(N, m, σ) in the "pure state" are not suitable for a practical construction of extended SAN(N) with a predefined fault-tolerance factor l=σ–1 using source SAN(m). In this case the needed PFNs don't exist or aren't constructed yet, or consist of enormous count of source SAN copies. Take the source SAN(16) as an example. Then, accordingly to Table 2, at $1 \le l \le 5$ there exist necessary PFNs, containing no less than 49 copies of the source SAN, but their state is unknown yet. For l=7 and l=9 the needed PFNs are nonexistent, while for l=6 and l=8 they consist of 31 and 25 source SAN copies, respectively.

3. FLAT SAN WITH PREDEFINED PARAMETERS

Creating acceptable extended SANs become feasible, if one can nest PFN(N, m, σ) into a set of source SAN(K) copies at $K \ge m$. It turns out that this is a quite easy procedure (Podlazov et al 2006a, b, 2007).

First of all, we shall consider a case of $K = rm$, where r is an integer. Let us take r copies of PFN(N, m, σ) and renumber them. Subscribers with numbers J ($0 \le J \le N-1$) are coupled to the zero PFN, as described in a previous section. Subscribers with numbers $J+jN$ are coupled to the j-th copy of PFN ($1 \le j < r$) in the same manner as subscribers with numbers J were coupled to the zero copy of PFN. As a result, subscribers with numbers $J+jN$ are coupled to the same copy of the source SAN at each given J. The extended SAN(R) created in the manner shown above comprises of N copies of the source SAN, unites $R=rN$ distinct subscribers and proves to be a flat network by construction.

The example of constructing the extended SAN(21) is given in Table 3. It is built up of 7 source SAN(12) copies using PFN(7, 4, 2). Copies of the source SAN are defined by table rows and PFN are emphasized by rectangular parts of the table in different prints.

Table 3. Extended flat SAN(21) built of 3 PFN(7, 4, 2). SAN(21) comprises of 7 copies of SAN(12). There are at least two parallel paths between any pair of subscribers.

Copies of the source SAN	Extended SAN											
	zero PFN				1st PFN				2nd PFN			
0	0	6	5	3	**7**	**13**	**12**	**10**	14	20	19	17
1	1	0	6	4	**8**	**7**	**13**	**11**	15	14	20	18
2	2	1	0	5	**9**	**8**	**7**	**12**	16	15	14	19
3	3	2	1	6	**10**	**9**	**8**	**13**	17	16	15	20
4	4	3	2	0	**11**	**10**	**9**	**7**	18	17	16	14
5	5	4	3	1	**12**	**11**	**10**	**8**	19	18	17	15
6	6	5	4	2	**13**	**12**	**11**	**9**	20	19	18	16

The following assertion is true for constructed extended SANs.

Assertion 2. Extended SAN(R) assembled of r PFN(N, m, σ) is a flat SAN($R=rN$) comprising of N copies of the source SAN(rm) in which between any pair of subscribers there exist σ or $m \ge \sigma$ parallel paths passing through distinct source SAN copies.

Proof. All results of Assertion 2, besides a count of parallel paths, follow immediately from constructing of the extended SAN.
Calculating the number of paths is based on the fact that each PFN copy consists of subscribers, whose numbers form modulo N residue ring.

Between subscribers of individual PFN whose numbers have distinct residues mod N there exist paths which pass only through the same copies of the source SAN as in a zero PFN. Between subscribers of different PFNs whose numbers have distinct residues mod N, there exist paths which again pass only through the same source networks as in a zero PFN. The number of such parallel paths equals σ.

Between subscribers of different PFNs whose numbers have the same residues mod N, there exist m distinct paths which pass through different copies of the source SAN. This follows from the fact that the said subscribers are coupled to the same copies of the source SAN, and each subscriber is coupled to m distinct copies of the source SAN.

Denote the extended SAN from Assertion 2 as ESAN(R, N, K, $m\backslash\sigma$). It has $R=NK/m$, and the following analog of Assertion 2 is valid for it.

Assertion 3. Any ESAN(R, N, K, $m\backslash\sigma$) proves to be (σ-1)-fault-tolerant by links.

At K=12 and m=4, accordingly to Table 2, it is possible to construct ESAN(21, 7, 12, 4/2), ESAN(15, 5, 12, 4\3), ESAN(12, 4, 12, 4\4). At K=12 and m=3 it is possible to construct ESAN(16, 4, 12, 3\2) and ESAN(12, 3, 12, 3\3). At K=12 and m= 6 it is possible to construct ESAN(32, 16, 12, 6\2), ESAN(22, 11, 12, 6\3), ESAN(14, 7, 12, 6\5) и ESAN(12, 6, 12, 6\6). Lastly, at K=12 and m=12 it is possible to construct ESAN(23, 23, 12, 6\6).

Even greater opportunities would arise when taking SAN's reduction as a source SAN. Based on reducing SAN(12) to SAN(10), it is possible to additionally construct ESAN(22, 11, 10, 5\2), ESAN(12, 6, 10, 5\4) and ESAN(10, 5, 10, 5\5) as well as ESAN(19, 19, 10, 10\5), ESAN(16, 16, 10, 10\6), ESAN(11, 11, 10, 10\9), and so on.

The example cited above shows that parameter values in ESAN(R, N, K, $m\backslash\sigma$) may be exchanged over a wide range.

Now return back to the case when m is not a devisor of K. Let r be a maximum integer for which $K > rm$, and let $K_0 = (r-1)m$. This case reduces to the previous one by reducing the source SAN(K) to SAN(K_0).

We shall seek a solution to a problem of constructing fault-tolerant-by-links ESAN with prescribed parameters in the statement as follows. Let we have the source SAN(K). For given $k \geq 0$ and $l \geq 1$, it is necessary to construct ESAN(R, N, K, $m\backslash\sigma$) with $\min R \geq K + k$, $\min \sigma > l$ and $\min N$.

This problem may be solved using the following procedure. First we seek admissible PFN(N, m, σ) for which $NK/m \geq K + k$ and $\sigma = l + 1$, to buildup of them a required ESAN. In so doing we shall restrict our search by considering only PFN on emphasized diagonals of Table 2, since all PFN are admissible there.

The first top diagonal is used only at k=0 and allows to construct ESAN using only PFN(σ, σ, σ). If $\sigma = l + 1$ and K=$r\sigma$, then it is possible to construct only a trivial ESAN(K, K, K, $\sigma\backslash\sigma$), defining a unique solution of the problem; otherwise there are no solutions.

The second diagonal allows using only PFN(σ+2, σ+1, σ) for ESAN construction. This diagonal is suitable for building ESAN in which $(\sigma + 2)K/(\sigma + 1) \geq K + k$. Here a solution is defined by selecting such $\sigma = l + 1$ for which the previous inequality is hold. If a solution exists, it will be ESAN($\lceil (\sigma+2)K/(\sigma+1) \rceil$, σ+2, K, (σ+1)\$\sigma$).

If there is no solution on the second diagonal, we seek it on the third one, where only PFN(4σ–1, 2σ, σ) are admissible for constructing ESAN, and where it is possible to construct only ESANs in which $(4\sigma - 1)K/(2\sigma) \geq K + k$. If a solution exists, it will be $\sigma = l + 1$ and ESAN($\lceil (4\sigma–1)K/(2\sigma) \rceil$, 4$\sigma$–1, K, 2$\sigma\backslash\sigma$).

Lastly, in the absence of solution on the third diagonal, we seek it on the fourth one, which allows the use of PFN(4σ+3, 2σ+1, σ) alone for constructing ESAN, and is suitable for creating ESANs in which $(4\sigma + 3)K/(2\sigma + 1) \geq K + k$. In this event, the solution is $\sigma = l + 1$ and ESAN($\lceil (4\sigma+3)K/(2\sigma+1) \rceil$, 4$\sigma$+3, K, (2σ+1)\$\sigma$).

When R or N values in a constructed ESAN(R, N, K, $m\backslash\sigma$) are too large, it is necessary to reduce the source SAN(K) to SAN(K–1) or take $\sigma = l + 2$ and repeat the constructing procedure.

Consider now several examples. Let K=32 at k=8 and l=2. Here, the solution ESAN(40, 5, 32, 4\3) is being constructed on the second diagonal. Let K=32 at k=8 and l=3. In that case the solution ESAN(40, 15, 32, 8\4) is being constructed on the third diagonal. Let K=32 at k=4 and l=3. In this situation one can increase the fault-tolerance factor up to l=7 or reduce SAN(32) to SAN(30), to obtain a solution on the second diagonal: ESAN(36, 9, 32, 8\6) and ESAN(36, 6, 30, 5\4), respectively. Lastly, let K=32 at k=6. Here, there are no solutions with R=38 on diagonals in Table 2. Because of this, we are obliged to restrict ourselves to abovementioned solutions with R=40.

Consider yet another example for K=80. Then at k=8, k=10, k=16 and k=20 there are the following solutions on the second diagonal: ESAN(88, 11, 80, 10\9), ESAN(90, 9, 80, 8\7), ESAN(96, 6, 80, 5\4), and ESAN(100, 5, 80, 4\3) with l=8, l=6, l=3 and l=2, respectively.

4. CONCLUSIONS

The present work proposes a method for constructing fault-tolerant system area networks for multiprocessor computer systems in the form of flat extended system area network. The flat system area network consists of multiple copies of the source system area networks. Any paths between any pair of processors as used here pass only through a single copy of the source system area networks. Extended networks may count more processors in comparison with the source network and have several paths between any pair of processors passing through distinct copies of the source network. The proposed method allows increase a number of processors and a count of parallel paths at specified values.

Flat extended system area networks can be treated also as system area networks with a predefined multiplicity of throughput increasing between any pair of processors. In this event, it is possible also to combine both approaches: some parallel paths are being used for increasing a throughput of the system area network while the remaining part serves for increasing its fault-tolerance by links. In this event, one can say already about multiprocessor system fault-tolerance and capacity management through a modular standby of a system area network.

One class of system area networks may be pointed out whereby flat extended system area networks allow constructing fault-tolerant multiprocessor systems with any predefined factors of fault-tolerance both by processors and by links – non-blocking system area networks. They provide for the same data communication delays between any points subscriber connection. In circuit switching, this class includes single-stage switches of sufficiently large sizes (Podlazov et al 2006a, b, 2007). In packet switching, this class includes multirings and hypercubes with conflict-free statical schedules (Podlazov 2001a, b) as well as switches with a Caley graph structure at block-sequential packet transmission (Podlazov 2003).

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