A NEW FRACTIONAL FREQUENCY SYNTHESIZER ARCHITECTURE WITH STABILITY AND ROBUSTNESS ANALYSIS

M. Houdebine [*,**] **S. Dedieu** [*] **M. Alamir** [**] **O. Sename** [**]

[*] *ST Microelectronics Crolles central R&D, 850 rue Jean Monnet, 38926 Crolles Cedex, FRANCE*
Email : {Marc.Houdebine, Sebastien.Dedieu}@st.com
[**] *Laboratoire d'Automatique de Grenoble, UMR CNRS-INPG-UJF 5528, ENSIEG-BP 46, 38402 Saint Martin d'Hères Cedex, FRANCE.*
Email: {Mazen.Alamir, Olivier.Sename}@inpg.fr

Abstract: This paper presents a new fractional frequency synthesizer architecture and its semi-global stability and robustness analysis tool. The proposed analysis tool takes into account the switched and non linear characteristics of the system components. In order to validate this study, simulation results were obtained with electronics simulators.

Keywords: Phase Locked Loop, Frequency Synthesis, Phase noise, Semi-Global Stability, Semi-Global robustness, Poincaré Map, hybrid model.

1. INTRODUCTION

Local oscillators are widely used in modern electronics for clock recovery, telecom modulation or demodulation, working from the lowest frequency ranges to the optical frequencies.
Since it is impractical to have too many different crystal oscillators, frequency synthesizers change a fixed frequency into a desired output frequency. These devices are based on Phase Locked Loop architectures (PLL) by locking a tunable oscillator to an accurate frequency source as a crystal oscillator.
In this paper, our aim is to design a low noise RF frequency synthesizer fully integrated on silicon working from 1.2GHz up to 2GHz for the Digital Video Broadcasting Television (DVBT). Because the output spectrum purity has to be optimum, classical structures are limited by their performances. The new frequency synthesizer presented in this paper is a solution for these performance limitations.
PLL stability is still a topical question especially because the challenge is to increase the loop bandwidth as far as possible while improving noise performances.
To study the stability of the loop, linear continuous models are mostly used providing a loop bandwidth much below than the sampling frequency fixed by the reference clock (Crawford, 1994)(Tang *et al.*, 2002) and restricting the analysis close to the operating point (Acco, 2001).
Some PLL also called Sampled Phase Locked Loop (SPLL) take advantage of the sampling but are prone to "False lock" by having unwanted stable states (Stensby, 2002), (Szabó and Kolumbán, 2003).
The structure presented in this paper is a noiseless fractional sampled frequency synthesizer for which we developed a stability and robustness analysis tool. Frequency synthesizer robustness analysis are mostly based on linear models (Holtzman *et al.*, 1999). In this paper, the developed tool takes into account the non-linear component characteristics and the system sampling.
The content of this paper is as follows. Classical structures and their limitations are described in section 2. Our new system is presented in section 3. Section 4 develops the new semi-global stability analysis tool. Some simulation results are depicted in section 5.

2. CLASSICAL PLL ARCHITECTURES

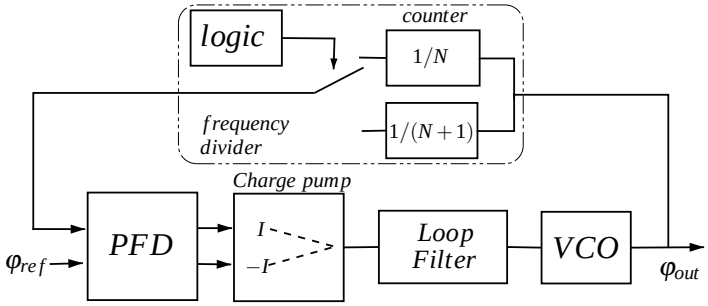

Fig. 1. Classical PLL scheme

Frequency synthesizers are based on Phase Locked Loops architectures composed of (see figure 1):

(1) The Phase Frequency Detector (PFD):
The digital PFD compares the reference phase delivered by a quartz component and the output phase divided by the feedback counter. It generates impulses whose width is proportional to the phase displacement. The two outputs are alternatively set to high logic level in case of lead or lag of the output phase in comparison with the reference phase.

(2) The charge pump and loop filter :
These cells work as a digital to analog converter. The charge pump produces two similar output currents. It sinks a current in while the down input is set to the high logic level and sources the same current when the up input is active. No current flows if both input are set to the same logic state.

(3) The loop filter integrates the charge pump current into the voltage command and ensures the loop stability.

(4) The Voltage Controlled Oscillator (VCO):
The VCO represents the process controlled by voltage. The output from the VCO is a periodic signal whose varying period makes the phase noise also called jitter. The VCO small signal model is frequency linear ($F_{out} = K_0\ V_0\ +\ F_0$) but large signal models have to consider variations in K_0 and F_0.

(5) Dividers :
Because electronic frequency dividers are period counters, only integer division by N ($N \in \mathbb{N}$) are possible with divider cells. To realize fractional ratios, a logic cell generates the sequence to select alternatively the $\frac{1}{N}/\frac{1}{N+1}$ counter output proportionally to the needed fractional part. By the loop filter, the average value corresponding to the fractional part is held at the VCO input.

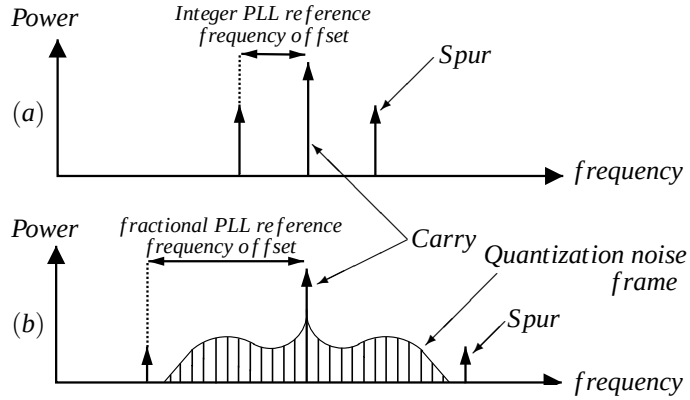

Fig. 3. Output spectrum: (a) Integer PLL, (b) fractional PLL.

Used as a frequency synthesizer, the PLL generates an accurate frequency (the carry in figure 3) from a given frequency delivered by the reference crystal oscillator ($F_{ref} = \dot{\varphi}_{ref} = \frac{1}{T_{ref}}$). The output frequency is higher than the reference frequency clock thanks to the divider placed on the feedback path.
In case of integer frequency ratio, a single programmable divider is needed. Then, the reference frequency corresponds to the output frequency step generated. For closer step, the reference frequency has to be low. To ensure the loop stability (Crawford, 1994), the loop bandwidth has to be small compared to the input frequency. As a result, the VCO noise is less filtered (Vaucher, 2002) (Kroupa, 2003) and the loop filter component dimension increases.
This problem does not occur in fractional division in which

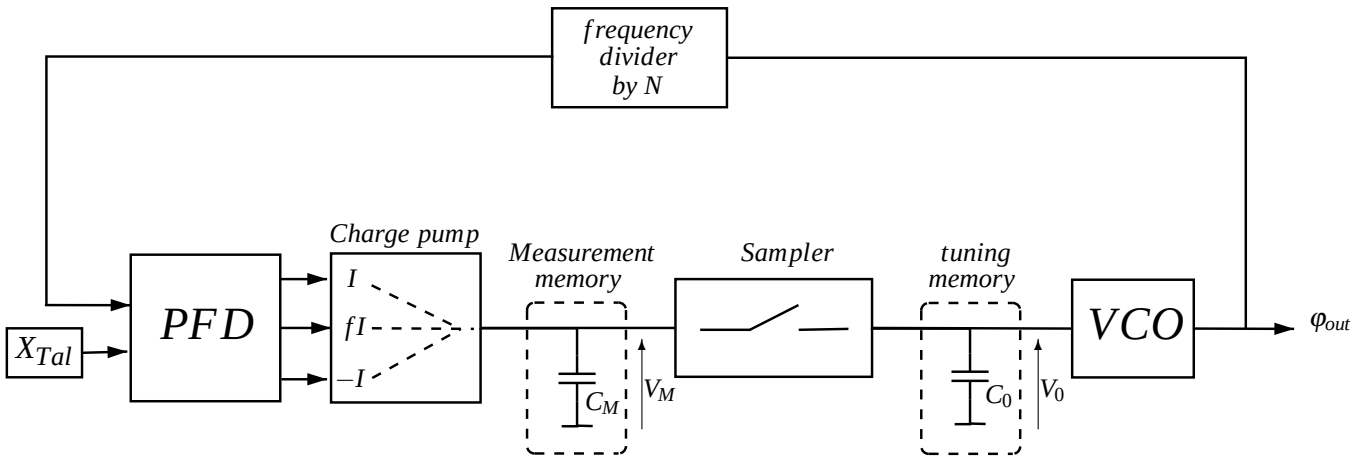

Fig. 2. New frequency synthesizer architecture

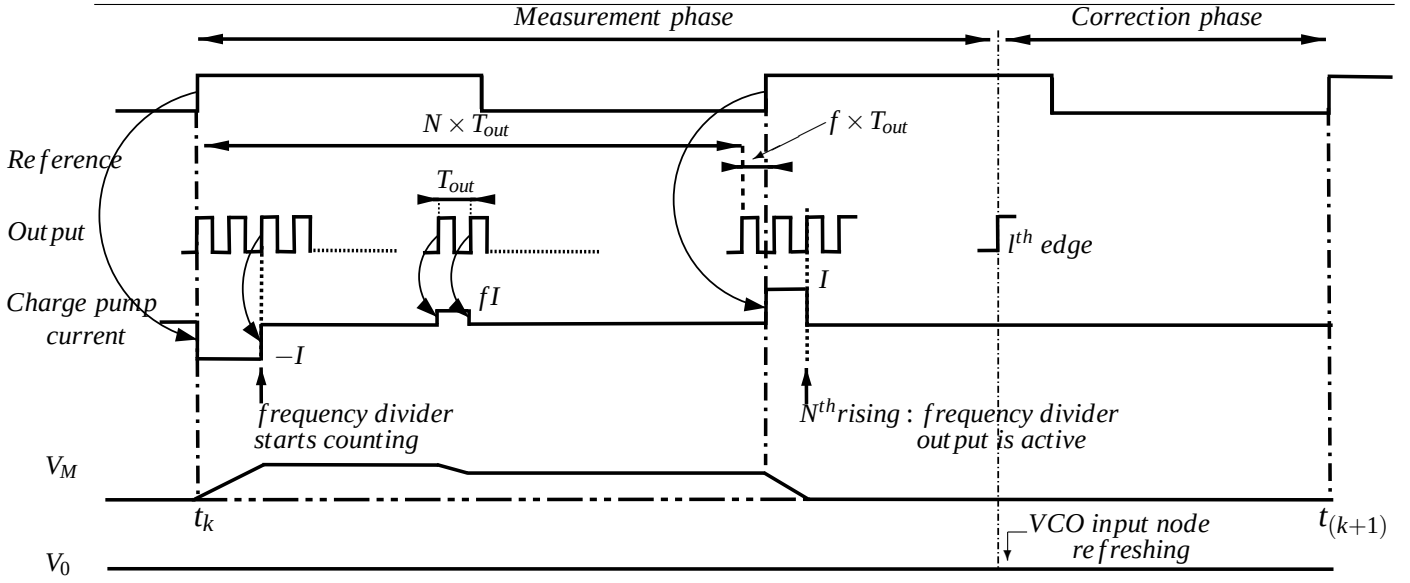

Fig. 4. System chronogram in phase lock case.

case the fractional part sets the minimal frequency step. This makes the usefulness of fractional divisions. In classical structures, fractional division is obtained by switching alternatively the output of two or more integer counters, but this modulation creates the quantization noise which gives spurious (see figure 3 (b)). Moreover, as shown in figure 3, spurs due to the VCO input refreshing are separated from the carry by the reference frequency value. In fractional PLL, these spurs are farther from the carry and better filtered. The new frequency synthesizer analysed in this paper is a fractional sampled PLL free from quantization noise. Yet, there are still two unavoidable spurs owing to the VCO tuning node refreshing at each sampled time. The reference frequency is chosen as high as possible to decrease the sample time in order to push aside these spurs from the carrier. Because two reference clock periods are needed to execute one sample time, the carry-spur spacing is equal to $F_{ref}/2$. Added to these spurs, additional rays are due to clock feedthrough of the sampling switch (Zhang *et al.*, 2003).

3. THE NEW FREQUENCY SYNTHESIZER ARCHITECTURE

The new frequency synthesizer architecture is shown in figure 2. To implement this quantization noise free fractional PLL (Joet *et al.*, 2002) (Houdebine and Dedieu, 2003), two phases are needed: output frequency measurement and VCO input voltage correction.

3.1 cycles of two phases

The system works by cycles of two phases. First, the output frequency measurement stores charges in the measurement capacitor C_M if the system is unlocked (see figure 2). Throughout the measurement phase, the opened sampler switch isolates the VCO from the measurement capacitor C_M. Capacitor C_0 keeps constant the tuning voltage maintaining the output frequency.
Then, by closing the sampler switch, the correcting phase adds the measurement charges ΔQ into the integration capacitor C_0. Close to the locking state, the VCO input voltage variation ΔV between two successive updates separated by two reference periods is proportional to the frequency error:

$$\Delta V = k\frac{I}{C_0}[(N+f)T_{out} - T_{ref}] = \frac{\Delta Q}{C_0} \qquad (1)$$

In the ideal case, $(N+f)T_{out} = T_{ref}$ at the steady state and $\Delta V = 0$.

3.2 Output frequency measurement

To generate a Giga-Hertz signal whose frequency is a reference real multiple, we take into account the integer part N and the fractional part f of the ratio separately

$$F_{out} = (N+f)F_{ref} \begin{cases} N \in \mathbb{N}. \\ 0 \leqslant f \leqslant 1. \end{cases} \qquad (2)$$

The integer part is loaded into the programmable frequency divider and the fractional part is set by a programmable charge pump. As shown in figure 4, to carry out the frequency measurement, the charge pump sinks and sources a nominal current I and supplies the fractional weighted current $f \times I$ thanks to a switchable elementary current sources array.
As shown in figure 4, to be insensitive to the cyclic phase displacement between the reference and the output phase involved by the fractional division, the measurement starts with a negative current from the reference rising edge to the second next VCO output rising. As a result, when the system is ideally locked, the injection error due to the counter lag is compensated and charges stored are equal to :

$$\Delta Q = (\tau_{lag} + 2T_{out})(-I) + fIT_{out} + (\tau_{lag} + (1-f)T_{out} + T_{out})I = 0. \quad (3)$$

Where T_{out} is the output period, I is the nominal current and τ_{lag} is the cyclical phase displacement due to the non-integer division. Indeed, contrary to integer division, when the system is locked, the time difference $f \times T_{out}$ prevents both input and output signal to be in phase at each measurement period. The $f \times I$ injection current is sinked anywhere during the measurement phase but away from the other injections to prevent any current interference.
As described in (Houdebine and Dedieu, 2003), this method casts off synchronisation delays, charge injection delay and injections disturbances.
Equation (3) validity domain corresponds to the linear ascendant part of the PFD saturated characteristic. The PFD transfer characteristic is saturated due to the measurement method: in case of large lead phase, the charge stocked in C_M equals $\Delta Q = (\tau_{lag} + 2T_{out})(-I) + fI$ and in case of large lag phase, the charges are equal to $\Delta Q = (l-1)T_{out}I$ where l is the limiting rising edge for realisability considerations.
Finally, contrary to classical PLLs, no dead zone affects this PFD thanks to the minimum injection time of one output period but this default could also be modeled in the analysis tool.

4. SYSTEM ANALYSIS

The stability/robustness analysis tool proposed here is based on the methodology described in (Chemori and Alamir, 2004). The method checks small signal stability as small signals models do but also the system convergence far from the operating point. This analysis is necessary to avoid oscillations, unstable states and false lock phenomena. Informations about convergence behavior can also be deduced, as well as robustness analysis w.r.t parameter variations.

4.1 General framework

The general theorem (Chemori and Alamir, 2004) is the following:

Theorem 1. Consider the discrete time dynamic equation:

$$V(k+1) = G(V(k), p) \quad (4)$$

$V \in \mathbb{R}^n$ is a state vector and $p \in \mathbb{R}^p$ is a parameter vector. If there exist real scalars $\rho_1,\ \rho_2$, some $\gamma \in [0,1[$ and $i \in \mathbb{N}$ such that

$$(a) \quad \sup_{\substack{\|V-V_d\| \leqslant \rho_i \\ p \in \mathbb{P}}} \|G(V,p) - V_d\| \leq \rho_i,\ i \in \{1,2\}$$
$$(b) \quad \sup_{\substack{\rho_1 \leqslant \|V-V_d\| \leqslant \rho_2 \\ p \in \mathbb{P}}} \|G^{(i)}(V,p) - V_d\| \leqslant \gamma \|V - V_d\| \quad (5)$$

Then, the neighborhood $B_{\rho_1} = \{V : \|V - V_d\| \leqslant \rho_1\}$ is attractive stable for all initial condition laying in B_{ρ_2} and all parameters p with values in $\mathbb{P}$. ♠

Sketch of the proof (see (Chemori and Alamir, 2004) for complete proof):

(1) if $V(0) \in B_{\rho_2}$ then $V(k) \in B_{\rho_2} \forall k$ by induction using (a) and (4).

(2) Assume $\rho_1 \neq 0$, $\exists \gamma,\ i$ s.t. :
$$\|V(qi) - V_d\| \leqslant \gamma \|V((q-1)i) - V_d\|$$
whenever $V((q-1)i) \in B_{\rho_2} \backslash B_{\rho_1}$, therefore $V(qi)$ can-not remain outside B_{ρ_1} indefinitely therefore B_{ρ_1} is attractive. Since it is also invariant thanks to (a) the theorem follows.

In the case $\rho_1 = 0$:
B_{ρ_1} is reduced to $\{0\}$ and the system clearly converges to the desired state vector V_d.

□

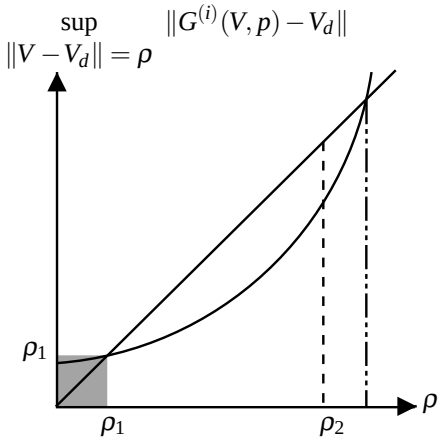

Fig. 5. Theorem 1 typical scenario

Figure 5 proposes a typical scenario where theorem 1 is valid. Region where the curve is under the first bisecting line induces a system evolution toward $\rho \leqslant \rho_1$. If the curve is above the first bisecting line, the system evolution will move away from V_d. In figure 5, if the curve leaves the grey square

(i.e. for $\|V - V_d\| < \rho_1$, if $\sup_{\|V-V_d\|=\rho} \|G^{(i)}(V,p) - V_d\| > \rho_1$),

oscillations might occur. This justifies the condition (a) with $i = 1$.
In the following simulations, for clarity we represent the ratio

$$\sup_{\|V-V_d\|=\rho} \left\{ \frac{\|G^{(i)}(V,p) - V_d\|}{\|V - V_d\|} \right\} \quad (6)$$

where the curve has to be lower than 1 between ρ_1 and ρ_2.

4.2 Application to the frequency synthesizer

In electronic frequency synthesizer, states are chosen among capacitor node voltages, current through inductors,

signal phase or any other varying state. In figure 4, state variable V_M checks the same value when the system is locked at each t_k corresponding to the end and begin of cycles. Because the VCO input voltage V_0 presents the same particularity, the instant t_k is a suitable Poincaré section (Hiskens, 2001) (Fujisaka and Sato, 1997) enabling the components of theorem 1 to be applied: $V(t_{k+1}) = G(V(t_k)) = V(t_k)\ with\ V = \begin{pmatrix} V_0 \\ V_M \end{pmatrix}$. $p \in \mathbb{P}$ is the parameters vector where $\mathbb{P}$ is the parameter space defined by manufacturing process mismatches. For stability analysis, $\mathbb{P}$ is reduced to the parameter nominal values. For robustness analysis, $\mathbb{P}$ is defined by all possible parameter values. The system equation G could be a piecewise defined non-linear function as well as a linear transforms composition.

5. SIMULATION EXAMPLES

The system description in section 3 shows the different non-linear bloc subsystems. The PFD and charge pump characteristic is saturated. The VCO characteristics take K_0 and F_0 variations thanks to a tanh expression. The sampling circuit non-linearity, offset variations and non-instantaneous charge transfer are also modeled. Two different simulations are presented, both of them with the same frequency synthesizer architecture but with different component values. In both cases, block transfer characteristics are identical; capacitors C_M, C_0 are respectively equal to $10pF$ and $30pF$, but the nominal current value supplied by the charge pump is firstly equal to $100\mu A$ and then to $130\mu A$ in the second simulation. Simulations were achieved with Spectre simulator and Cadence tools (figures 6 and 9).

In both cases, classical small signal analysis asserts that the loop is stable. However, these exemples show that False lock can happen in the first case (figure 6).

Figure 6 represents six time system evolutions with different initial states. Three of them lead to a false lock state. This phenomenon is detected in figure 7 where expression (6) crosses 1 for all i. The corresponding point gives the distance ρ_{FL} between the false lock state and the desired state V_d. The analysis tool (figure 7) indicates $\rho_{FL} = 0.225$ corresponding to an output frequency error of 4.3MHz what electronics simulations confirm (figure 6). The region of attraction for this point corresponds to the area where expression (6) is placed above 1 closer to V_d and under 1 farther from V_d. Any simulation starting from this region will converge to the false lock state.

To avoid any false lock or instabilities, component values are chosen thanks to the analysis tool. Figure 8 shows the analysis tool results for $I = 130\mu A$. Increasing the charge pump current of $30\mu A$ ensures the loop stability within $B_{0.7}$. Electrical simulations in figure 9 confirm this stability for some initial conditions. It is worth noting that stability results of figure 8 are hold for all any initial conditions in $B_{0.7}$ but not only for figure 9 initial states.

For robustness analysis, the parameter space $\mathbb{P}$ takes the component variation values into account: VCO gain K_0

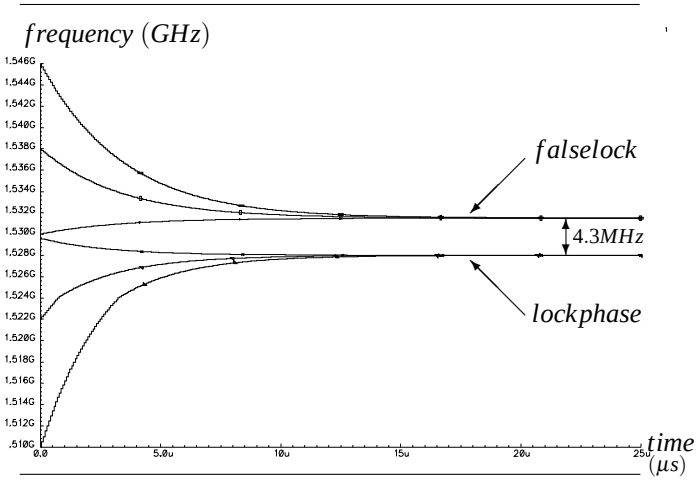

Fig. 6. System evolution in a False Lock case ($I = 100\mu A$)

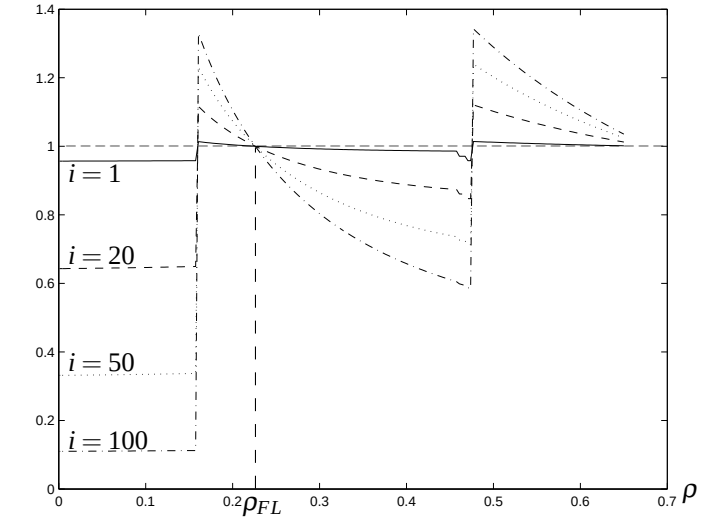

Fig. 7. analysis tool result for $I = 100\mu A$

variations are about 80%, current variations 10% and capacitor variations 20%. For simplicity, Figure 10 shows the robustness analysis with $p = I$ and $\mathbb{P} = [120\mu A,\ 140\mu A]$ but the parameter vector could also have been: $p = \{I,\ K_0,\ F_0,\ C_M,\ C_0\}$. The results show that $I = 130\mu A$ is the optimal current value to ensure the loop robustness in spite of process mismatch.

6. CONCLUSION

The free from quantization noise fractional frequency synthesizer architecture presented in this paper is a non-linear switched system. A semi-global analysis tool was developed to study the system stability and robustness. The sampling clocked by the reference frequency is convenient to find the most appropriate Poincaré section. The new system off-line analysis ensures robustness in order to avoid false lock state, divergence, instabilities or any other

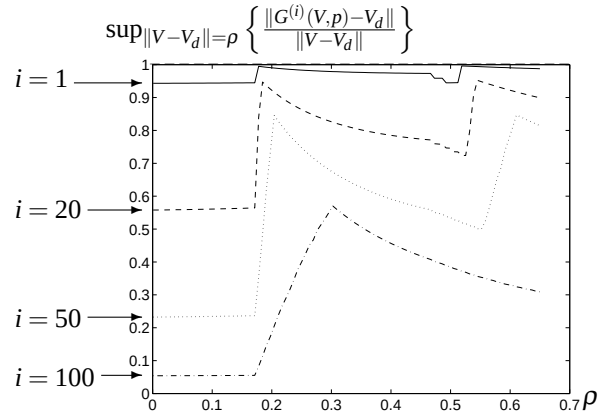

Fig. 8. Analysis results for $I = 130\mu A$

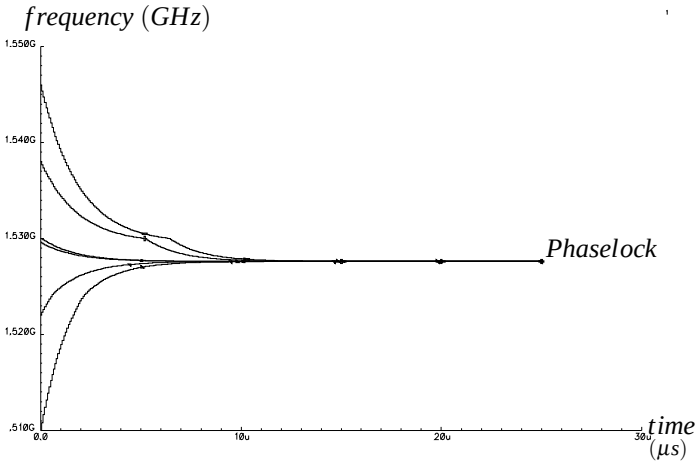

Fig. 9. Ideal stability case ($I = 130\mu A$)

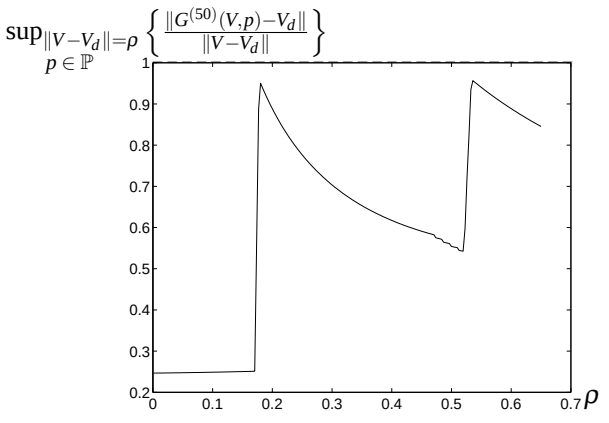

Fig. 10. Robustness analysis results for $p = I$; $\mathbb{P} = [120\mu A, 140\mu A]$(see theorem 1).

problem inherent in classical Sampled PLL.

Thanks to this analysis tool, simulation time is saved and only worst cases are simulated. The analysis results were successfully compared with electronic simulations and soon compared with measurements.

REFERENCES

Acco, P. (2001). Why do we linearise charge pump pll equations so early ?. In: *Nonlinear Dynamics of Electronic Systems NDES'01*. Delft, The Netherlands.

Chemori, A. and M. Alamir (2004). Generation of multi-steps limit cycles for rabbit using a low dimensional (scalar) nonlinear predictive control scheme. *IEEE/RSJ international conference on Intelligent Robots and Systems, Sendai, Japan*.

Crawford, James A. (1994). *Frequency Synthesizer Design Handbook*. ArtechHouse Boston.London.

Fujisaka, H. and C. Sato (1997). Computing the number, location, and stability of fixed points of poincaré maps. *IEEE, Transactions on circuits and systems-I: Fundamental theory and applications* **44**(4), 303–311.

Hiskens, Ian A. (2001). Stability of hybrid system limit cycles: Application to the compass gait biped robot. *Proceedings of the 40th IEEE Conference on Decision and Control* pp. 774–779.

Holtzman, M., M. S. Fadali, B. Johnson and L. Lautzenhiser (1999). Robust stability analysis of phase-locked loop voltage-controlled oscillator circuit. *Proceedings of the American Control Conference* pp. 425–429.

Houdebine, M. and S. Dedieu (2003). Wide band and high frequency spectral purity fractional frequency locked loop. STM patent pending.

Joet, L., S. Dedieu, E. André and D. Saias (2002). Method and device for generating a signal with a frequency equal to the product of a reference frequency and a real number. Patent US2004113665.

Kroupa, Věnceslav F. (2003). *Phase Lock Loops and frequency synthesis*. Wiley.

Stensby, J. (2002). Stability of false lock states in a class of phase-lock loops. *IEEE, Proceedings of the Thirty-Fourth southeastern Symposium on System Theory* pp. 133–137.

Szabó, Zoltan and G. Kolumbán (2003). How to avoid false lock in spll frequency synthesizers. *IEEE Transactions on instrumentation and measurements* **52**(3), 927–931.

Tang, Y., M. Ismail and S. Bibyk (2002). A new fast-settling gearshift adaptative pll to extend loop bandwidth enhancement in frequeny synthesizers. *IEEE, International Symposium on circuits and systems* **4**, IV–787 – IV–790.

Vaucher, Cicero S. (2002). *Architectures for RF frequency synthesizers*. Kluwer Academic Publisher.

Zhang, B., E. Allen and J. M. Huard (2003). A fast switching pll frequency synthesizer with an on-chip passive discrete-time loop filter in $0.25 - \mu m$ cmos. *IEEE, journal of solid state circuits* **38**(6), 855–865.