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# Performance Evaluation of Battery Balancing Hardware

Matthias Preindl, Claus Danielson, and Francesco Borrelli

***Abstract*— In this paper we evaluate the performance of seven proposed hardware topologies for balancing the cells in a battery pack. We consider four classes of battery balancing hardware; shunting, cell-to-stack, storage element, and dissipative hardware. We present models of these hardware topologies that capture the steady-state behavior of the balancing hardware dynamics. We evaluate the hardware topologies based on time required to balance the cells and energy dissipated during balancing. A linear programming based method for calculating the worst-case time to balance and energy dissipated during balance is provided. The number of linear programs required to compute both metrics grows exponentially with the number of cells. We show how to use symmetries to efficiently compute both metrics. Our approach scales well for large-scale battery packs and provides non intuitive solutions.**

## I. Introduction

Electric and hybrid vehicles require battery systems with high voltage, high efficiency, and long lifetime [1], [2]. Battery cells are connected in series to provide the required voltage and efficiency. However, this setup leads to a nearly exponential reduction of the battery life as the string length increases [3], [4]. The lifetime reduction is mainly caused by charge imbalances of the cells, which worsen over time. Imbalances arise from internal and external effects. Internal effects include manufacturing variance, variations in internal impedance and different self-discharge rate. External effects include unequal draining due to protection circuits, and temperature variations between cells which alter internal impedance and self-discharge rates [5]. Cell imbalance reduces the effective capacity of the battery pack. Li-Ion battery cells require a balancing system to correct these cell imbalances.

There are two classes of battery balancing hardware; *dissipative* and *redistributive*. In dissipative balancing excess charge is drawn from the cells with the highest state-of-charge and dissipated through a shunt resistor. Redistributive balancing uses power electronics to move charge between cells [6], [7]. Redistributive balancing methods can further be distinguished by the operation principle used to move charge between the cells. In this paper we distinguish *shunting*, *cell-to-stack*, and *storage-element* methods. Shunting methods move charge between adjacent cells. Cell-to-stack methods move charge from a cell to the entire battery pack or vice-versa. storage-element methods use a passive storage element (capacitor or inductor) as an intermediary for moving charge between cells.

The battery balancing hardware designs we consider are described in detail in [5], [8]–[10]. The balancing hardware designs are evaluated in terms of *time-to-balance* and *energy-loss-to-balance*. Time-to-balance is the minimum time required for any controller to balance the cells from a given initial imbalance. Energy-loss-to-balance is the minimum energy dissipated for any controller when balancing a given initial cell imbalance. In practice the time-to-balance and energy-dissipated-to-balance will depend not only on the hardware design but also on the controller design and initial cell imbalance. In our study, we remove dependencies on control design and initial cell imbalance in the following way: the hardware designs are evaluated in terms of best-case controller performance for the worst-case initial conditions.

The time-scale of cell balancing is typically measured in hours. Therefore our models neglect the fast dynamics of the power electronics [11], [12] and internal battery chemistry [13], [14]. We model the battery cells using simple continuous-time integrator dynamics. The cells are able to exchange charge through balancing hardware [15]. We assume that the state-of-charge of the battery cells is available. Details on estimating the state-of-charge for battery cells can be found in [16]–[20].

The number of linear programs required to compute the time-to-balance and energy-loss-to-balance metrics grows exponentially with the number of cells. We show how to use symmetries to efficiently compute both metrics. Our approach scales well with the number of battery cells and allows us to compute the performance metrics for large scale battery packs. We use simulations with high fidelity power electronic models and to show the effectiveness of our approach.

## II. Battery System

The amount of charge stored in the battery cells is $Q_x x(t) \in \mathbb{R}^n_+$ where $x \in [0,1]^n \subseteq \mathbb{R}^n_+$ is the normalized state-of-charge of the cells and the diagonal matrix $Q_x \in \mathbb{R}^{n\times n}_+$ contains the charge capacities of the battery cells. State-of-charge is the amount of stored charge normalized by the total charge capacity of the cell. A state-of-charge of $1$ corresponds to the full battery cell and $0$ corresponds to a empty cell.

The state-of-charge of the battery cells is controlled through the balancing current $Q_u u(t) \in \mathbb{R}^m_+$ where $u(t) \in [-1,1]^m$ is the normalized balancing current and the diagonal matrix $Q_u \in \mathbb{R}^{m\times m}_+$ contains the current capacities of the balancing hardware.

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M. Preindl is with University of Padua, via Gradenigo 6/A, 35131 Padua, Italy (+39-049-8277590; matthias.preindl@gmail.com)

C. Danielson is with University of California Berkeley, 6141 Etcheverry Hall, Berkeley, CA 94720-1740 (claus.danielson@me.berkeley.edu)

F. Borrelli is with University of California Berkeley, 6141 Etcheverry Hall, Berkeley, CA 94720-1740 (fborrelli@berkeley.edu)

The state-of-charge and balancing current are related by the integrator dynamics

$$Q_x \dot{x}_i(t) = T Q_u u(t) \tag{1}$$

where the topology matrix $T$ relates the balancing currents and state-of-charge. The topology matrix $T$ depends on the balancing hardware topology. In Section III we will define the balancing topology matrices $T$ for the hardware topologies considered in this paper. For notational simplicity we write the dynamics as

$$\dot{x}(t) = Bu(t) \tag{2}$$

where $B = Q_x^{-1} T Q_u \in \mathbb{R}^{n \times m}$. The state-of-charge can be expressed explicitly in terms of the control input,

$$x(\tau) = x(0) + B \int_0^\tau u(t) dt. \tag{3}$$

The state-of-charge and normalized balancing current are constrained by

$$x(t) \in \mathcal{X}, \ u(t) \in \mathcal{U} \tag{4}$$

for all $t \in \mathbb{R}_+$ where $\mathcal{X} = [0,1]^n$ and the input constraints $\mathcal{U} \subseteq [-1,1]^m$ depend on the hardware topologies described in Section III.

### A. Battery Balancing Problem

In this section we define the control objectives for battery balancing.

The battery balancing problem involves finding a balancing current trajectory that balances the battery cells. We define the set of balanced states as

$$\bar{\mathcal{X}} = \left\{ x \in \mathbb{R}^n | \ x_i = x_j \ \forall i,j \in [1,...,n] \right\} \subseteq \mathcal{X} \tag{5}$$

In a balanced state the amount of charge that can be removed from the battery pack and amount of charge that can be added to the battery pack are both maximized [15]. The battery balancing problem is formally defined below.

**Problem 1** (Battery Balancing)**.** Find a terminal time $\tau$ and input trajectory $u(t)$ for $t \in [0,\tau]$ such that $x(t) \in \mathcal{X}$ and $u(t) \in \mathcal{U}$ for all $t \in [0,\tau]$, and $x(\tau) \in \bar{\mathcal{X}}$.

Before continuing we prove two results that simplify the battery balancing problem. Proposition 1 shows that the infinite dimensional problem of finding an input trajectory $u(t)$ can be transformed into a finite-dimensional problem.

**Proposition 1.** *There exists an input trajectory $u(t)$ for $t \in [0,\tau]$ that solves Problem 1 if and only if there exists a constant input trajectory $u(t) = \bar{u} \in \mathcal{U}$ for $t \in [0,\tau]$ such that*

$$x(\tau) = x(0) + B\bar{u}\tau \in \bar{\mathcal{X}}. \tag{6}$$

*Proof.* First we prove the existence of a trajectory $u(t)$ for $t \in [0,\tau]$ that solves Problem 1 implies the existence of a constant trajectory $\bar{u} \in \mathcal{U}$. Let

$$\bar{u} = \frac{1}{\tau} \int_0^\tau u(t) dt. \tag{7}$$

Then $\bar{u}$ satisfies (6). Furthermore $\bar{u} \in \mathcal{U}$ since $u(t) \in \mathcal{U}$ for all $t \in [0,\tau]$, $\mathcal{U}$ is convex, and the integral is the limit of Riemann sums.

Now we prove the existence of $\bar{u}$ implies the existence of a trajectory $u(t)$ for $t \in [0,\tau]$ that solves Problem 1. Let $u(t) = \bar{u}$ for $t \in [0,\tau]$ then $u(t)$ satisfies $u(t) \in \mathcal{U}$ and $x(\tau) \in \bar{\mathcal{X}}$. Furthermore $x(t) = x(0) + B\bar{u}t \in \mathcal{X}$ for all $t \in [0,\tau]$ since $\mathcal{X}$ is convex and $x(0) + B\bar{u}\tau \in \bar{\mathcal{X}} \subset \mathcal{X}$. □

Next we show the set inclusion condition (6) can be replaced by an equality constraint. Therefore we have the equivalent simplified statement of the battery balancing problem.

**Proposition 2.** *Problem 1 can be solved by computing a terminal time $\tau$ and constant input trajectory $\bar{u} \in \mathcal{U}$ such that*

$$Lx(0) + LB\bar{u}\tau = 0. \tag{8}$$

*Proof.* Let $L = I - \frac{1}{n}\mathbf{1}\mathbf{1}^T$ then $x \in \bar{\mathcal{X}}$ if and only if $Lx = 0$ for any $x \in \mathcal{X}$. □

## III. Hardware Topologies

In this section we model the battery balancing hardwares presented in [5], [8]–[10]. First, the topologies are modeled based on the buck-boost and flyback converter topology [11], [12]. We are concerned with modeling the behavior of the balancing hardware over long time-scales relative to the dynamics of the power electronics and battery chemistry. Each hardware topology is modeled using the generic model (2) and (4) where the topology matrix $T$ and polytopic input constraint set $\mathcal{U}$ vary between hardware topologies. Many of the active balancing hardware topologies we present have passive counter-parts. In this paper we only consider active balancing hardware. However, the active topologies often provide an upper-bound on the performance of their passive counter-parts.

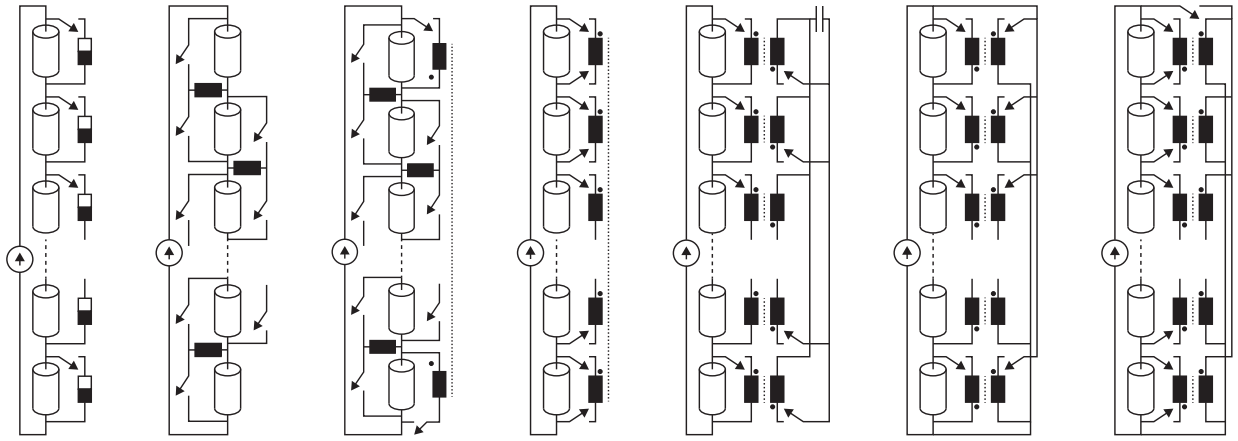
### A. Dissipative Topology

The dissipative topology is shown in Figure 1(a). In the dissipative topology charge is removed from cells with high state-of-charge and dissipated as waste heat. Examples of dissipative topologies are the dissipative resistor and dissipative shunting topologies from [5], [8]–[10]. In the dissipative shunting topology each cell has an independently actuated shunt circuit. The topology matrix $T$ is given by

$$T = \begin{bmatrix} -1 & 0 & 0 & ... & 0 & 0 \\ 0 & -1 & 0 & ... & 0 & 0 \\ 0 & 0 & -1 & ... & 0 & 0 \\ & & & ... & & \\ 0 & 0 & 0 & ... & -1 & 0 \\ 0 & 0 & 0 & ... & 0 & -1 \end{bmatrix} \in \mathbb{R}^{n \times m}$$

where $n$ is the number of cell and $m = n$ is the number of dissipative links. The input $u$ is limited by peak current constraint of the links $|u_i| \leq 1$ and since the topology is dissipative we have $u_i \geq 0$ for each $i = 1,2,...,m$. Therefore the input constraint set is

$$\mathcal{U} = \left\{ u \in \mathbb{R}^m \ | \ 0 \leq u_i \leq 1 \right\} \subseteq [0,1]^m.$$



(a) Dissip. (b) Line (c) Ring (d) Induct. (e) Capacitive (f) Individual (g) Common

Fig. 1. Balance hardware topologies: dissipative (a); line shunting (b); ring shunting (c); inductive storage element (d); capacitive storage element (e); individual cell to stack (f); common cell to stack (g)

### B. Shunting Topology

The shunting topologies are shown in Figure 1. In the line topology shown in Figure 1(b) charge is moved between neighboring cells in the series connection using buck-boost converters. In the ring topology shown in Figure 1(c) the first and last cells in the stack are connect to form a ring using a flyback converter. Examples of shunting topologies are the controlled shunting and switched capacitor topologies from [5], [8]–[10]. The topology matrix $T$ for the line shunting topology is given by

$$T = \begin{bmatrix} 1 & 0 & 0 & \dots & 0 & 0 \\ -1 & 1 & 0 & \dots & 0 & 0 \\ 0 & -1 & 1 & \dots & 0 & 0 \\ & & & \dots & & \\ 0 & 0 & 0 & \dots & -1 & 1 \\ 0 & 0 & 0 & \dots & 0 & -1 \end{bmatrix} \in \mathbb{R}^{n \times m}$$

where $n$ is the number of battery cells and $m = n - 1$ is the number of links. The ring shunting topology has the topology matrix

$$T = \begin{bmatrix} 1 & 0 & 0 & \dots & 0 & -1 \\ -1 & 1 & 0 & \dots & 0 & 0 \\ 0 & -1 & 1 & \dots & 0 & 0 \\ & & & \dots & & \\ 0 & 0 & 0 & \dots & 1 & 0 \\ 0 & 0 & 0 & \dots & 0 & 1 \end{bmatrix} \in \mathbb{R}^{n \times m}$$

where $n$ is the number of battery cells and $m = n$ is the number of links. The input $u$ is limited by peak current constraint of the links $|u_i| \leq 1$ for $i = 1, 2, ..., m$. Therefore the input constraint set is

$$\mathcal{U} = \left\{ u \in \mathbb{R}^m \mid -1 \leq u_i \leq 1 \right\} = [-1, 1]^m.$$

### C. Storage Element Topology

The storage element topologies are shown in Figure 1. In these topologies a passive storage element (capacitor or inductor) provides temporary storage for moving charge between cells. In Figure 1(d) the temporary storage element is an inductor and we use the multiple-winding inductor converter. In Figure 1(e) the temporary storage element is a capacitor and the links a realized with flyback converters. In both topologies the charge level of the storage element remains constant. Examples are the single switched capacitor topology and the multiple-winding inductor topology [5], [8]–[10]. The topology matrix $T$ for both the inductive and capacitive storage element topologies is given by

$$T = \begin{bmatrix} 1 & 0 & 0 & \dots & 0 & 0 \\ 0 & 1 & 0 & \dots & 0 & 0 \\ 0 & 0 & 1 & \dots & 0 & 0 \\ & & & \dots & & \\ 0 & 0 & 0 & \dots & 1 & 0 \\ 0 & 0 & 0 & \dots & 0 & 1 \end{bmatrix} \in \mathbb{R}^{n \times m}$$

where $n$ is the number of cells and $m = n$ is the number of links. The input constraint sets are different for the capacitive and inductive storage element topologies. In both variants the input $u$ is limited by peak current constraint of the links $|u_i| \leq 1$ for $i = 1, 2, ..., m$. Since the storage element should neither be charged nor discharged over time, we have the addition constraint $\sum_{i=1}^{n} Q_{u,i} u_i = 0$. Therefore the input constraint set of the capacitive storage element topology is

$$\mathcal{U} = \left\{ u \in \mathbb{R}^m \mid -1 \leq u_i \leq 1 \text{ and } \textstyle\sum_{i=1}^{m} Q_{u,i} u_i = 0 \right\}.$$

In the inductive topology (Figure 1(e)) only one link can be active at each time instant. This constraint can be satisfied by ensuring that the total control action is less than one at each time instant $\|u\|_1 \leq 1$. Therefore the input constraint set of the inductive storage element topology is

$$\mathcal{U} = \left\{ u \in \mathbb{R}^m \mid -1 \leq u_i \leq 1, \textstyle\sum_{i=1}^{m} Q_{u,i} u_i = 0, \|u\|_1 \leq 1 \right\}.$$

### D. Cell to Stack Topology

The cell-to-stack topologies are shown in Figure 1. In these topologies, charge is removed from one cell and distributed equally among all the cells in the stack. Likewise charge can be drawn equal from all the cells and added to a single cell. We consider two variants of the cell-to-stack topology; the common cell-to-stack topology shown in Figure 1(f), which uses a converter with parallel mutual inductors, and the individual cell-to-stack topology shown in Figure 1(g), which uses flyback converters. In the latter each cell has an individual link to the stack that can be operated independently from the other cells. This requires more high voltage switches but allows simultaneous movement of charge to and from

multiple cells. Examples of the cell-to-stack topologies are the single and multiple transformer topologies from [5], [8]–[10]. The topology matrix $T$ for the cell-to-stack topologies is given by

$$T = \begin{bmatrix} \frac{1}{n}-1 & \frac{1}{n} & \frac{1}{n} & \dots & \frac{1}{n} & \frac{1}{n} \\ \frac{1}{n} & \frac{1}{n}-1 & \frac{1}{n} & \dots & \frac{1}{n} & \frac{1}{n} \\ \frac{1}{n} & \frac{1}{n} & \frac{1}{n}-1 & \dots & \frac{1}{n} & \frac{1}{n} \\ & & & \dots & & \\ \frac{1}{n} & \frac{1}{n} & \frac{1}{n} & \dots & \frac{1}{n}-1 & \frac{1}{n} \\ \frac{1}{n} & \frac{1}{n} & \frac{1}{n} & \dots & \frac{1}{n} & \frac{1}{n}-1 \end{bmatrix} \in \mathbb{R}^{n\times m}$$

where $n$ is the number of cells and $m = n$ is the number of links. We use the sign convention $u_i > 0$ to indicate charge flow from cell $i$ to the stack and $u_j < 0$ to indicate charge flowing from the stack to the $j$-th cell. The input constraint sets are different for the individual and common cell-to-stack topologies. In both the input $u$ is limited by peak current constraint of the links $|u_i| \leq 1$ for $i = 1, 2, ..., m$. Therefore the input constraint set of the individual cell-to-stack topology is

$$\mathcal{U} = \big\{u \in \mathbb{R}^n \mid -1 \leq u_i \leq 1\big\}.$$

In the common cell-to-stack topology only one link can be active at each time instant $\|u\|_1 \leq 1$. Therefore the input constraint set of the common cell-to-stack topology is

$$\mathcal{U} = \big\{u \in \mathbb{R}^n \mid -1 \leq u_i \leq 1 \text{ and } \|u\|_1 \leq 1\big\}.$$

## IV. Performance Metrics

In this section we define the metrics used to evaluate the performance of the hardware topologies described in Section III. In practice hardware performance will depend on the control design and initial imbalance as well as the hardware design. Our performance metrics are defined such that they are independent of controller design and initial conditions. The performance metrics depend only on the hardware design.

### A. Time to Balance

The time-to-balance $\tau^\star$ is the minimum amount of time required to equalize the state-of-charge of the battery cells. The dependency of the time-to-balance on the initial condition $x(0)$ is removed by considering the worst-case time-to-balance over a set of initial imbalances $\mathcal{D} \subseteq \mathcal{X}$. The dependency on the controller design is removed by consider the best-case performance for any controller. The time-to-balance is defined in Definition 1.

**Definition 1.** Let $\mathcal{D} \subseteq \mathcal{X}$ be a set of initial cell imbalances. The time-to-balance $\tau^\star$ is

$$\tau^\star(\mathcal{D}) = \operatorname{argmin}\{\tau \in \mathbb{R}_+ \mid \forall x(0) \in \mathcal{D},\, \exists u(t) \in \mathcal{U}\ \forall t \in [0,\tau] \text{ s.t. } x(t) \in \mathcal{X} \text{ and } x(\tau) \in \bar{\mathcal{X}}\} \tag{9}$$

Proposition 3 provides a procedure for calculating the time to balance for a given polytopic set of initial imbalances $\mathcal{D} \subseteq \mathcal{X}$.

**Proposition 3.** *Let $\mathcal{U} = \{u \mid Hu \leq K\}$ and let $\mathcal{D} = \operatorname{conv}\{\hat{x}_1, \dots, \hat{x}_r\}$. The time-to-balance can be computed as*

$$\tau^\star(\mathcal{D}) = \max_{i\in\{1,\dots,r\}} \tau_i^\star \tag{10}$$

*where*

$$\begin{aligned} \tau_i^\star = \underset{\tau\geq 0, v}{\text{minimize}} \quad & \tau && \text{(11a)} \\ \text{subject to} \quad & L\hat{x}_i + LBv = 0 && \text{(11b)} \\ & Hv - K\tau \leq 0 && \text{(11c)} \end{aligned}$$

*for each vertex $\hat{x}_i$ of $\mathcal{D} = \operatorname{conv}\{\hat{x}_1, \dots, \hat{x}_r\}$ and where $L = I - \frac{1}{n}\mathbf{1}\mathbf{1}^T$.*

*Proof.* In Proposition 2 we showed that there exists an input trajectory $u(t) \in \mathcal{U}$ for $t \in [0, \tau]$ such that $x(t) \in \mathcal{X}$ and $x(\tau) \in \bar{\mathcal{X}}$ if and only if there exists a constant trajectory $v \in \mathcal{U}$ such that $Lx + \tau LBv = 0$. Thus for any $x \in \mathcal{D}$ the time-to-balance is

$$\begin{aligned} \tau^\star(x) = \underset{\tau\geq 0, v}{\text{minimize}} \quad & \tau && \text{(12a)} \\ \text{subject to} \quad & Lx + LBv = 0 && \text{(12b)} \\ & Hv - K\tau \leq 0 && \text{(12c)} \end{aligned}$$

where $v = \tau\bar{u} \in \tau\mathcal{U}$. For any $x \in \mathcal{D}$ the value function $\tau^\star(x)$ provides a lower-bound on the worst-case time-to-balance $\tau^\star(\mathcal{D}) \geq \tau^\star(x)$. Since the value function $\tau^\star(x)$ is convex [21] the maximum occurs at one of the vertices of the set $\mathcal{D}$. □

Calculating the time-to-balance $\tau^\star(\mathcal{D})$ for a given polytopic set $\mathcal{D}$ requires solving the linear program (11) for each vertex of the polytope $\mathcal{D}$. It is well known that the number of vertices grow exponentially in the dimension of the polytope [22]. However in special cases the time-to-balance can be calculated more efficiently by exploiting the symmetry of the hardware topologies.

**Theorem 1.** *Let $\mathcal{D} = \{x \in \mathcal{X} \mid \|Lx\|_\infty \leq d\}$ and let $Q_x = q_x I_n$ be the cell charge capacities and $Q_u = q_u I_m$ the link current capacities. Then the time-to-balance can be calculated by solving the linear program (11) for the $n-1$ points*

$$L\hat{x}_i = d\begin{bmatrix}\mathbf{1}_{n-k} \\ -\mathbf{1}_n\end{bmatrix} \tag{13}$$

*for $k = 1, \dots, n-1$ where $d \in [0, 0.5]$ is the worst-case imbalance for each battery cells.*

*Proof.* Proposition 3 states that the worst-case time-to-balance can be calculated by evaluating $\tau^\star(x)$ at each vertex of $\mathcal{D}$ where $\tau^\star(x)$ is the solution to the linear program (12).

It can be shown that the value function $\tau^\star(x)$ is invariant under permutations $\tau^\star(P_n x) = \tau^\star(x)$ for any permutation matrix $P_n \in \mathbb{R}^{n\times n}$. Thus the time-to-balance $\tau^\star(x)$ is constant for each vertex in the vertex orbit

$$\mathcal{O}(x_i) = \big\{P_n\hat{x}_i \mid P_n\big\} \subset \big\{\hat{x}_1, \dots, \hat{x}_r\big\} \tag{14}$$

where $\mathcal{D} = \operatorname{conv}\{\hat{x}_1, \dots, \hat{x}_r\}$. Therefore the number of linear programs we must solve to calculate the worst-case time-to-balance is equal to the number of vertex orbits of the set $L\mathcal{D}$.

The parameter set $\mathcal{D}$ can be written as $\mathcal{D} = \mathcal{C} \oplus d\mathcal{H}$ where $\mathcal{C} \subset \operatorname{null}(L)$, $\mathcal{H} = \{x \mid \|x\|_\infty \leq 1\}$ is a hyper-cube, and $\oplus$ is the Minkowski sum of sets. Thus $L\mathcal{D} = dL\mathcal{H}$. Hyper-cubes have $n+1$ vertex orbits; all vertices with $k$ ones and $n-k$ negative ones are equivalent under permutation. The vertices $\mathbf{1}$ and $-\mathbf{1}$ are mapped to the origin under $L = I - \frac{1}{n}\mathbf{1}\mathbf{1}^T$. This leaves the $n-1$ vertices in equation (13) that must be checked. □

### B. Energy Dissipated to Balance

The energy-dissipated-to-balance $\varepsilon^\star$ is the minimum amount of energy dissipated in the process of balancing the battery cells. Each charge transfer $u(t)$ dissipates a portion of the stored energy. The power dissipation is a non-linear function of the voltage and current [23], [24]. However in practice the power electronics are operated about a single current set-point. Furthermore the voltage range of the battery cells is limited and can be upper-bounded. Therefore we assume the energy dissipation is directly proportional to the magnitude of the control action according to the relation

$$\varepsilon(u) = \int_0^\tau \|Wu(t)\|_1 dt \tag{15}$$

where $W$ is a diagonal matrix which defines the dissipation of the links. Realistic efficiency ranges were obtained from [23], [24].

In order to remove the dependency on the initial imbalance we consider the worst-case energy dissipation over a set of initial imbalances $\mathcal{D} \subseteq \mathcal{X}$. The dependency on the controller design is removed by consider the best-case performance for any controller. The energy-dissipated-to-balance is defined in Definition 2.

**Definition 2.** Let $\mathcal{D} \subseteq \mathcal{X}$ be a set of initial cell imbalances. The energy-dissipated-to-balance is

$$\varepsilon^\star(\mathcal{D}) = \max_{x\in\mathcal{D}} \min_{\tau,u(t)} \quad \int_0^\tau \|Wu(t)\|_1 dt \tag{16a}$$

$$\text{subject to} \quad Lx + LB\int_0^\tau u(t) = 0 \tag{16b}$$

$$u(t) \in \mathcal{U},\ x(t) \in \mathcal{X}\ \forall t \in [0,\tau]$$

Proposition 4 provides a procedure for efficiently calculating the energy-dissipated-to-balance for a given polytopic set of initial imbalances $\mathcal{D} \subseteq \mathcal{X}$.

**Proposition 4.** *Let $\mathcal{U} = \{u | Hu \le K\}$ and let $\mathcal{D} = \text{conv}\{\hat{x}_1, \dots, \hat{x}_r\}$. Then the energy-dissipated-to-balance is given by*

$$\varepsilon^\star(\mathcal{D}) = \max_{i\in\mathcal{I}(\mathcal{D})} \ \varepsilon_i^\star \tag{17}$$

*where*

$$\varepsilon_i^\star = \underset{\tau\ge 0, v}{\text{minimize}} \quad \|Wv\|_1 \tag{18a}$$

$$\text{subject to} \quad L\hat{x}_i + LBv = 0 \tag{18b}$$

$$Hv - K\tau \le 0 \tag{18c}$$

*for each vertex $\hat{x}_i$ of $\mathcal{D} = \text{conv}\{\hat{x}_1, \dots, \hat{x}_r\}$ and where $L = I - \frac{1}{n}\mathbf{1}\mathbf{1}^T$.*

*Proof.* In Proposition 2 we showed that there exists an input trajectory $u(t) \in \mathcal{U}$ for $t \in [0,\tau]$ such that $x(t) \in \mathcal{X}$ and $x(\tau) \in \bar{\mathcal{X}}$ if and only if there exists a constant trajectory $\bar{u} \in \mathcal{U}$ such that $Lx + \tau LB\bar{u} = 0$. Furthermore the constant trajectory $\bar{u}$ has a lower cost than an equivalent general trajectory $u(t)$ since

$$\|W\bar{u}\tau\| = \Big\| \int_0^\tau Wu(t)dt \Big\| \le \int_0^\tau \|Wu(t)\| dt \tag{19}$$

for any norm $\|\cdot\|$ and weighting matrix $W$. Thus for any $x \in \mathcal{D}$ the energy-dissipated-to-balance is

$$\varepsilon^\star(x) = \underset{\tau\ge 0, v}{\text{minimize}} \quad \|Wv\|_1 \tag{20a}$$

$$\text{subject to} \quad Lx + LBv = 0 \tag{20b}$$

$$Hv - K\tau \le 0 \tag{20c}$$

where $v = \tau\bar{u} \in \tau\mathcal{U}$. For any $x \in \mathcal{D}$ the value function $\varepsilon^\star(x)$ provides a lower-bound on the worst-case energy-dissipated-to-balance $\varepsilon^\star(\mathcal{D}) \ge \varepsilon^\star(x)$. Since value function $\varepsilon^\star(x)$ is convex [21] the maximum occurs at one of the vertices of the set $\mathcal{D}$. □

Calculating the energy-to-balance $\varepsilon^\star(\mathcal{D})$ for a given polytopic set $\mathcal{D}$ requires solving a linear program for each vertex of the polytope $\mathcal{D}$. It is well known that the number of vertices grow exponential in the dimension of the polytope [22]. However in special cases the energy-dissipated-to-balance can be calculated more efficiently by exploiting the symmetry of the hardware topologies.

**Theorem 2.** *Let $\mathcal{D} = \{x \in \mathcal{X} \mid \|Lx\|_\infty \le d\}$ and let $Q_x = q_x I_n$ be the cell charge capacities and $Q_u = q_u I_m$ the link current capacities. Then the energy-dissipated-to-balance can be calculated by solving the linear program (18) for the $n-1$ points*

$$L\hat{x}_i = d\begin{bmatrix}\mathbf{1}_{n-k} \\ -\mathbf{1}_n\end{bmatrix} \tag{21}$$

*for $k = 1, \dots, n-1$ where $d \in [0, 0.5]$ is the worst-case imbalance for each battery cells.*

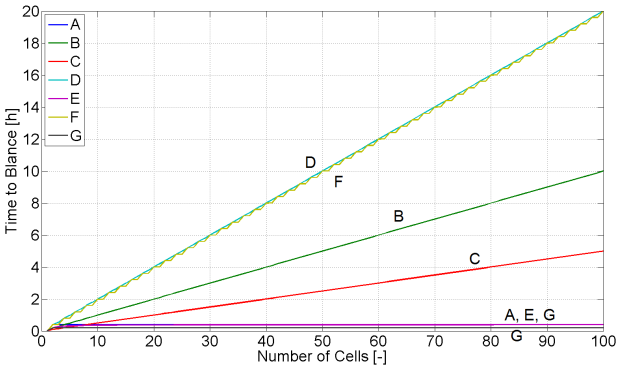
*Proof.* The proof of Theorem 4 is similar to the proof for Theorem 3. □

## V. Results

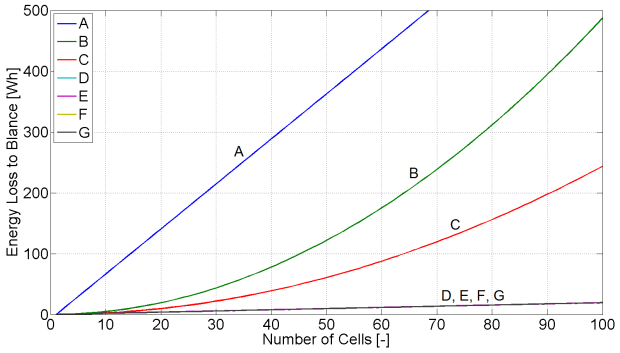
In this section we demonstrate our methodology for an example battery pack. For this example the charge capacity of the battery cells is 10[A-h], the current capacity of the links is 5[A], and the rated voltage per cell is 3.7[V]. Thus, $W = 18.5 I_m$[Wh] for dissipative topologies. For the non-dissipative hardware topologies, we assume 95% link efficiency, which results in $W = 0.974 I_m$[Wh]. The initial imbalances are $\pm 10\%$ from balance $\mathcal{D} = \{x \mid \|Lx\|_\infty \le 0.1\}$. We show the time-to-balance $\tau^\star(\mathcal{D})$ and energy-dissipated-to-balance $\varepsilon^\star(\mathcal{D})$ as function of the battery pack size $n$ for different hardware topologies. We vary $n$ of the battery pack between 2 and 100 battery cells.

The dissipative hardware topology (trajectory A in Figure 2) is widely used in industry and it is used as a benchmark reference. Figure 2(a) shows that the time-to-balance for dissipative topologies is not sensitive to the battery pack size $n$. The worst-case time-to-balance remains constant regardless of the number of cells $n$. However Figure 2(b) shows that the energy-dissipated-to-balance increases drastically with battery pack size $n$.

The shunting topologies (trajectory B and C in Figure 2) move charge between adjacent cells arranged in a string or ring formation. Figure 2(a) shows that the time-to-balance grows linearly with the number of cells $n$. Figure 2(b)




(a) Time to balance $\tau^\star(\mathcal{D})$




(b) Energy-loss-to-balance $\varepsilon^\star(\mathcal{D})$

Fig. 2. Topologies: A dissipative, B line shunting, C ring shunting, D inductive storage element, E capacitive storage element, F common cell-to-stack, G individual cell-to-stack

shows that the energy-dissipated-to-balance grows exponentially with the number of cells $n$. Compared to the other hardware topologies, the shunting topologies have poor time-to-balance and energy-dissipation. This behavior is a result of the fact that charge cannot be moved directly from an arbitrary cell $i$ to another $j$. Instead the charge must move through all the intermediate cells in the string or ring.

The storage element topologies (trajectory D and E in Figure 2) use a capacitive or inductive storage element to move charge directly between any cells. In the capacitive topology charge can be moved between several cells simultaneously. In the inductive topology charge can only be moved between two cells at each time instant. As a results the time-to-balance for the capacitive topology is independent of the number of cells in the pack $n$ as shown in Figure 2(a). On the other hand the time-to-balance for the inductive topology grows linearly with the number of cells $n$. The time-to-balance of the inductive topology has the highest rate of grow or the seven topologies. Figure 2(b) shows that the energy-dissipated-to-balance grows linearly with the number of cells $n$ in the battery pack. The rate of grow of the storage element energy-dissipated-to-balance is among the lowest of the seven topologies.

The cell-to-stack topologies (trajectory F and G in Figure 2) move charge between individual cells and the entire cell stack. If the links can be used simultaneously the time-to-balance is constant as shown in Figure 2(a). On the other hand, if only one link can be used at each time instant then the time-to-balance grows linearly with the number of cells. The energy-dissipated-to-balance grows linearly with the number of cells $n$ as shown in Figure 2(b). Both time-to-balance and energy-dissipated-to-balance have a similar rate of grow than the storage element topologies.

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