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ELECTRICAL PARAMETER CONTROL FOR SEMICONDUCTOR DEVICE MANUFACTURING: A FABWIDE APPROACH

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Abstract: Wafers that fail to meet their electrical specifications lead to scrap which negatively impacts yield and manufacturing costs. Most existing research has focused on controlling individual steps during the manufacturing process via run-to-run control, but almost no work has looked at directly controlling the electrical characteristics. A control scheme is proposed to directly control electrical parameter values. The control algorithm uses a model to predict electrical parameter values after each processing step and determines optimal adjustments for the future processing steps. Simulation results show significant reduction in electrical parameter variations for both constrained and unconstrained control.

Keywords:
hierarchical control, multi-step controllers, least squares estimation

1. INTRODUCTION

The semiconductor manufacturing industry is constantly faced with the challenge of producing ever-smaller devices to reduce manufacturing cost, improve product functions, and maintain competitiveness. This goal has necessitated the move from 200mm to 300mm wafers where manufacturing efficiency can be improved and manufacturing cost per unit area of silicon can be reduced. In order to justify the capital expenditures for 300mm fabrication facilities, maintaining operational efficiency and equipment utilization is critical. In the mean time, the critical dimensions of VLSI devices keep shrinking, making it a constant challenge to improve yields and throughput. Two factors that affect yield, cycle time, and manufacturing costs are wafers that need to be reworked and wafers that need to be scrapped. At the end of up to 300 processing steps, electrical test data is taken for each wafer and it is used to determine if wafers should be scrapped. Since electrical parameter values directly affect yield, controlling the electrical parameter variation is an important part of the manufacturing process.

The semiconductor manufacturing process consists of a series of discrete processes, each of which determines various wafer critical dimensions, film thickness, or doping concentrations etc. Each

piece of processing equipment has embedded real-time control to carry out a manufacturing specification. Most of the processing steps, each composed of multiple processing tools, are equipped with in-line metrology that measures the geometric properties of each processed feature. Run-to-run (R2R) control is usually implemented using in-line metrology (May and Spanos, 2006; Edgar *et al.*, 2000; Moyne *et al.*, 2001) After this series of processing steps is completed electrical properties are measured.

Much of the research in semiconductor manufacturing has focused on run-to-run control strategies that seek to maintain the critical dimensions at specified values by adjusting the recipes for the discrete processes. Geometric variables, such as critical dimensions, directly impact electrical parameters, therefore the use of R2R controllers to reduce variability in wafer critical dimensions has been a useful method for indirectly controlling electrical parameters. However, R2R controllers do not control every variable exactly on its target. Poorly tuned controllers, switching between products, and metrology errors all contribute to the manufacturing errors at each processing step. As a result, small errors in each processing step can accumulate in up to 300 processing steps to produce large errors and even off-specification products in terms of electrical parameters.

To avoid the accumulation of errors across many manufacturing steps coordination and the sharing of information among these sequential steps must be considered. Despite all of the research in semiconductor manufacturing control, very little work has closely examined the coordination of multiple processing steps to reduce variability and improve overall quality, in terms of electrical parameters. (Qin and Sonderman, 2002) first proposed a fab-wide control framework that aims to control the final electrical properties at the supervisory control level. (Harrison *et al.*, 2003) present a detailed strategy for electrical parameter control (EPC) of a flash memory device. (Qin *et al.*, 2004; Moyne, 2004; Qin *et al.*, 2006) further specify a three-level hierarchical control framework for fab-wide control. This paper discusses a fab-wide electrical parameter control strategy that uses measurements of critical dimensions from each processing step and a process model relating critical dimensions to electrical parameters to determine optimal set-points for later processing steps. This paper demonstrates the use of regression models built from experimental and historical data to predict electrical parameter values and shows the algorithm's effectiveness at controlling multiple outputs with and without constraints. Inspired from a real case study at a major semiconductor manufacturer, the impact of model quality on control of the electrical parameters is investigated.

2. ELECTRICAL PARAMETER CONTROL

The EPC scheme is a higher level of control that coordinates the lower level R2R controllers with the goal of reducing electrical parameter variation. R2R control at each processing step can achieve optimality for each step in the manufacturing process but that does not guarantee the optimality of the final output. A move from process-oriented R2R control to fab-wide control that integrates lower- level R2R controllers would allow the end-of-the-line goals to be optimized. Another advantage of a fab-wide control scheme is the ability to compensate for metrology drifts and systematic errors. R2R controllers are effective at compensating for equipment drift but they cannot compensate for metrology drifts (Del Castillo and Hurwitz, 1997). A block diagram showing how the fab-wide controller integrates with the existing R2R controllers is shown in Figure 1.

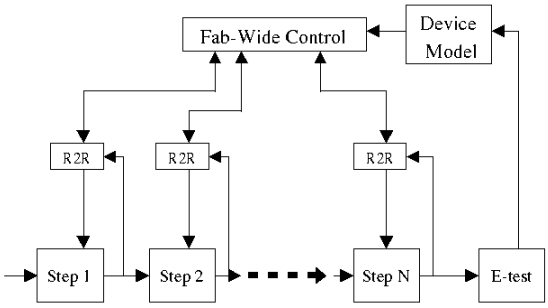

Fig. 1. Fab-wide control block diagram integrating electrical test data and R2R controllers

2.1 EPC Algorithm

This EPC algorithm takes a device model for the device being manufactured and metrology data from completed processing steps and uses this information to predict the electrical parameter values for the wafers currently being processed. Based on the predicted electrical parameter values, optimized targets for the subsequent processing steps are determined to ensure that the wafers meet all of the electrical parameter requirements at the end of processing. The optimized targets are the set points for lower-level R2R controllers and they are calculated by minimizing the difference between the predicted and targeted electrical parameter values according to the objective function:

$$\min_{\hat{u}} \|(y_t - f(\hat{u_2}, u_1)\|^2 + \lambda \|\hat{u_2} - u_{2,nom}\|^2 \quad (1)$$

$$s.t. \quad u_{2,min} \leq \hat{u_2} \leq u_{2,max}$$
$$y_{min} \leq f(\hat{u_2}, u_1) \leq y_{max}$$

Here vector y_t contains the desired electrical parameter values, u_1 represents the input values for completed processing steps, $\hat{u_2}$ represents the input values for subsequent processing steps, and λ is a weighting factor. The constraints set the appropriate lower and upper limits for $\hat{u_2}$. The variable being optimized is $\hat{u_2}$. The predicted electrical parameter values are obtained from the function, f, which is a model relating electrical parameters to input parameters, u_1 and $\hat{u_2}$. The model is discussed in more detail in Section 2.2. The second term in the objective function penalizes large changes in the input values, so that the input targets will not change drastically between groups of wafers that are processed. This helps produce stable targets for the lower-level R2R controllers. The constraints and target values can be specified by product specifications and requirements or they can be user determined values that are reasonable for the process. The target re-optimization occurs after new metrology data is measured for each processing step so only the most recent optimized target gets used. It is not necessary to calculate optimized targets for all of the subsequent processing steps but it allows the adjustments made at each step to be smaller because no one step is attempting to bring the outputs back on target.

2.2 Modeling

The EPC algorithm uses a model to predict electrical parameter values with data collected from completed processing and to determine the optimal set points for the future processing steps. First principles models and data driven models such as ordinary least squares and partial least squares may be used with this algorithm. The computation time to solve the minimization increases with the complexity of the model so complex first principles models for device design may not be appropriate. A regression model based on historical and experimental data is used for this paper because detailed knowledge of the semiconductor device structure and processing is not needed for modeling. Specific semiconductor device information is difficult to obtain and often proprietary so regression models are an attractive method for modeling in this situation.

The model used is a simple linear model of the form:

$$y = \theta x + \varepsilon \tag{2}$$

Where x is the $n \times 1$ input matrix, y is the $m \times 1$ output vector, ε is the model residual vector, and θ is the $m \times n$ regressed parameter vector. To estimate the model parameters θ, data in x and y from experimental design and historical operations can be used to obtain least squares estimates. Extensions of the ordinary least squares problems, partial least squares, can be used. The ordinary least squares solution is chosen for this paper because of its simplicity and it adequately demonstrates the benefits of the EPC algorithm. When using model (2) for EPC the input matrix x is partitioned into completed steps, u_1, and subsequent steps, $\hat{u_2}$. Also autoregressive and moving average models can be used with this algorithm but that is not addressed in this paper.

2.3 Disturbance Modeling

Process disturbances, such as drift, need to be compensated for in order to keep the process mean at target. This is accomplished by adding a term to the predictive model. The term is a weighted sum of the difference between the predicted and actual electrical values and the previous value of the constant.

$$\hat{y}_k = \theta x_k + d_k + \varepsilon \tag{3}$$

where

$$d_k = \lambda d_{k-1} + (1-\lambda)\frac{1}{w}\sum_{i=1}^{w}(y_i - \hat{y}_i) \tag{4}$$

where w is the number of lots that have completed processing before the coefficient is calculated and k is the number of processing steps before electrical test data is collected. Equation (4) is also known as an exponentially weighted moving average (EWMA) filter which comes from an IMA(1,1) disturbance model.

3. SIMULATION

3.1 Simulation Description

To evaluate the effectiveness of the algorithm a semiconductor fabrication process was simulated and various test cases were run. The simulated fab process has 13 processing steps and 4 outputs. The simulation is a two layer process where data for the 13 processing steps are generated using a R2R control simulation and data for the four electrical parameters is generated in a fabrication simulation using the R2R simulation data. At each step the R2R control simulation includes an IMA(1,1) disturbance, metrology error, and R2R controller model error. The fabrication simulation generates electrical parameter data using a linear model relating the 13 inputs to the four outputs. Normally distributed measurement error and an IMA(1,1) disturbance are added to the electrical parameters. The error standard deviations are

Table 1. Simulation Errors

Type	Error
Metrology Error	0.015
R2R Controller Parameter Error	2.0 %
Electrical Parameter Measurement Error	0.1

shown in Table 1 and a block diagram describing the simulation and added noise is shown in Figure 2.

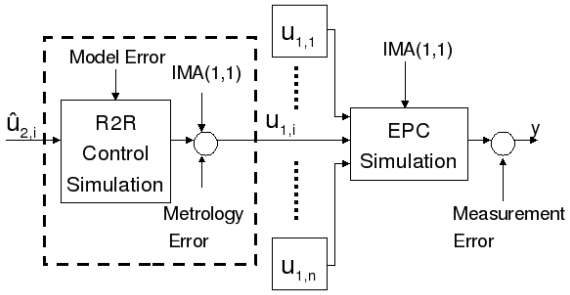

Fig. 2. Block diagram of simulation data and noise

The EPC algorithm requires a process model, so the simulation is run without the controller turned on to generate a training data set. A process model is derived from the training data set as described in Section 2.2 of this paper. This ensures that the model used for simulating the process and the model used for control are not the same. To demonstrate the effects of offset disturbances and constraints on controller performance different combinations of disturbances and constraints were used. These test cases are described in Section 3.2. Models with low R^2 values are used since it is difficult to obtain industrial data with better correlations. The model correlations are shown in Table 3. To demonstrate the effects of model quality on controller performance three test cases with models of varying quality and no constraints or offset disturbances were simulated. The model correlations and results are summarized in Table 2. In a real fabrication process adjustments can not be made at every step so in this simulation, adjustments can be made at all processing steps except the 1st and the 4th steps.

3.2 Simulation Results

The results of the model quality study are shown in Table 2. The simulation included an IMA(1,1) disturbance and process noise. It was run 100 times and the mean and standard deviation values for Y1, Y2, Y3, and Y4 were averaged. This study indicates that the model quality significantly impacts the algorithms effectiveness but even when using models with R^2 values on the order of 0.6 - 0.7 output variations can be reduced.

Table 2. Model quality effects on controller performance

	Output	R^2 Value	STD Improvement
Case 1	Y1	0.63	21.9 %
	Y2	0.64	21.2 %
	Y3	0.70	26.5 %
	Y4	0.73	28.5 %
Case 2	Y1	0.81	43.0 %
	Y2	0.82	43.6 %
	Y3	0.85	49.6 %
	Y4	0.87	49.0 %
Case 3	Y1	0.99	74.5 %
	Y2	0.99	75.4 %
	Y3	0.99	78.7 %
	Y4	0.99	79.3 %

The simulation used to evaluate the EPC algorithm performance with offset disturbances and constraints tested four test cases. Case 1 shows performance in the presence of the IMA(1,1) disturbance and process noise, Case 2 shows performance in the presence of the IMA(1,1) disturbance, process noise, and a metrology offset of 0.008 in the 2nd step and -0.008 in the 4th processing step, Case 3 is the same as Case 1 except that the controller constrains the calculated set point value, $\Delta\hat{u}_k = \hat{u}_k - \hat{u}_{k-1}$, and the difference between the last set point and the calculated set point value, and Case 4 applies the same constraints to Case 2. The constraints for Cases 3 and 4 are

$$-0.035 \leq \hat{u} \leq 0.035$$

$$-0.02 \leq \Delta\hat{u}_k \leq 0.02$$

The simulation was run 100 times and the mean and standard deviation values for Y1, Y2, Y3, and Y4 were averaged. A summary of this data is shown in Table 3. Figures 3-6 show a sample output for each case. The first 100 data points are the training data set and the second 100 data points show the improvement after the controller has been turned on. For all 4 cases the EPC algorithm kept the outputs very close to their set point values of 0 and significantly reduced variations in the outputs as shown by the reduction in standard deviation values. As expected the controller is less effective when constraints are in place as indicated by less improvement in the standard deviation for Cases 3 and 4 as compared to Cases 1 and 2 respectively.

4. INDUSTRIAL APPLICATION

Industrial data obtained from Texas Instruments is used to further demonstrate the effectiveness of the EPC algorithm. The data set used consists of 13 input variables, such as gate lengths and doping concentrations, and four outputs variables, such as parametric transistor drive current and leakage current. The data is taken when no inline set points are manipulated with a supervisory

Table 3. Output mean and standard deviation improvements with control

		R^2	Mean	STD Improvement
Case 1	Y1	0.63	-0.039	21.9 %
	Y2	0.64	-0.034	21.2 %
	Y3	0.70	-0.043	26.5 %
	Y4	0.73	-0.031	28.5 %
Case 2	Y1	0.63	0.032	17.6 %
	Y2	0.64	0.029	21.0 %
	Y3	0.70	0.0086	24.1 %
	Y4	0.73	0.026	27.1 %
Case 3	Y1	0.63	-0.042	9.0 %
	Y2	0.64	-.04	12.0 %
	Y3	0.70	-0.053	14.1 %
	Y4	0.73	-0.023	16.7 %
Case 4	Y1	0.63	-0.047	10.8 %
	Y2	0.64	-0.052	13.8 %
	Y3	0.70	-0.052	15.8 %
	Y4	0.73	-0.028	19.8 %

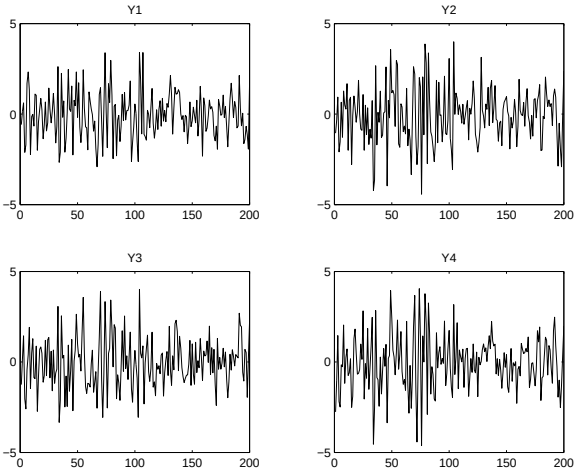

Fig. 3. Case 1 - IMA(1,1) disturbance and process noise

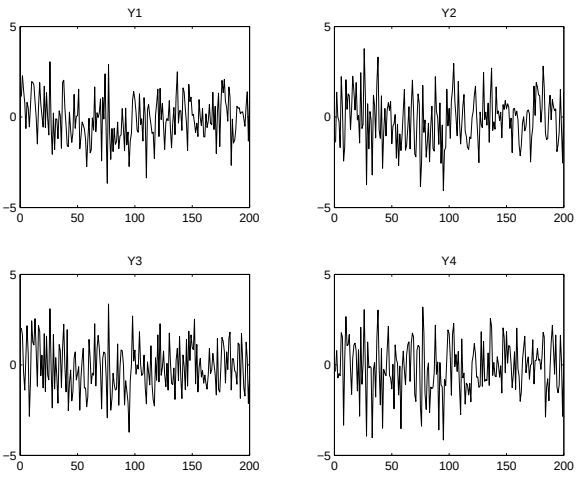

Fig. 4. Case 2 - IMA(1,1) disturbance, process noise, and metrology offset at Steps 2 and 4

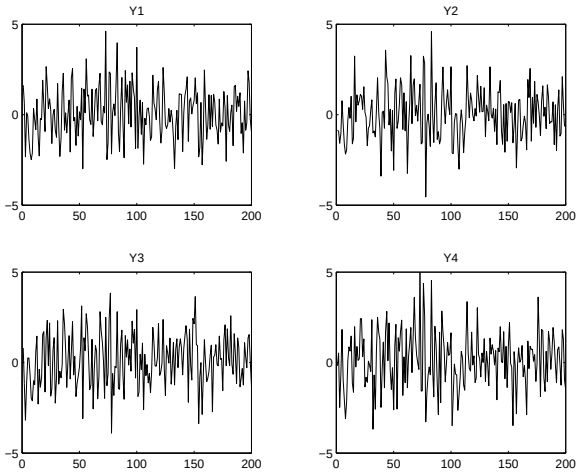

Fig. 5. Case 3 - IMA(1,1) disturbance and process noise with constraints on the manipulated variable

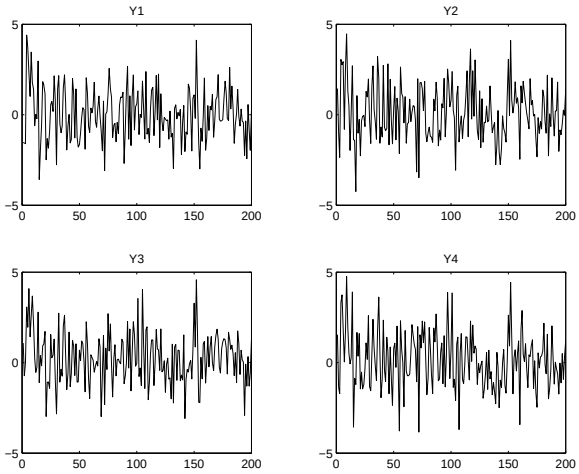

Fig. 6. Case 4 - IMA(1,1) disturbance, process noise, and metrology offset at Steps 2 and 4 with constraints on the manipulated variable

controller and the data is modeled using ordinary least squares. To determine the change in the process output values with EPC applied, the difference between the actual set point and the optimized set point calculated by the controller is multiplied by the corresponding coefficient in the least squares model. For this particular process the controller was only allowed to determine the set point for the 13th step of the process. Results are summarized in Table 4. Figure 7 shows the N channel leakage current values before and after control is applied. The horizontal lines indicate the standard deviation before and after control is applied. The data shows that the EPC algorithm effectively reduces the output variation in all four process outputs.

This industrial example is still an idealized case since real production fabs have multiple products running on multiple tools and metrology delay impedes the access to real time information. In a real manufacturing environment a different model

Table 4. Industrial Data Improvements

Output	STD no control	STD with EPC
Y1	1.0	0.70
Y2	1.0	0.63
Y3	1.0	0.77
Y4	1.0	0.74

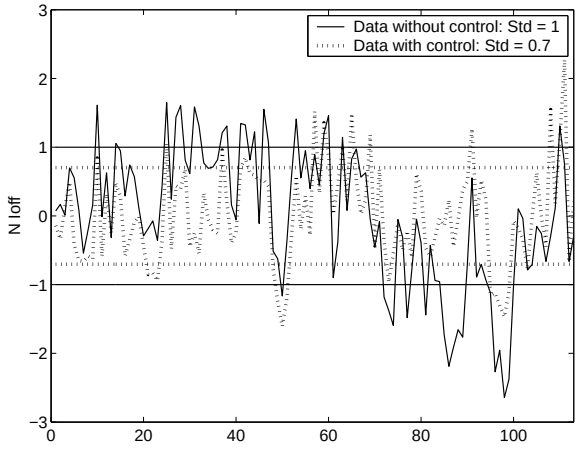

Fig. 7. Industrial Data with and without control

would be required for each product and various tool offsets and biases would need to be kept track of and included in the models. If a processing step has metrology delay the process target or average value can used for prediction purposed until the data becomes available.

5. CONCLUSION

The proposed EPC algorithm demonstrates the ability to maintain multiple output targets while reducing output variations in the face of disturbances, process noise, and metrology offsets. The algorithm can be used with or without constraints and a simple linear regression model is adequate for control. This algorithm directly controls electrical parameters and shows promise as supervisory controller that can be integrated into semiconductor manufacturing to help achieve desired electrical properties. Electrical test delay in the EPC framework will be investigated in the future.

6. ACKNOWLEDGMENTS

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