High-performance, microscale field-effect transistors for the probing of charge transport in molecular crystals

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Abstract

Organic single crystals have emerged as powerful tools for the exploration of the intrinsic charge transport properties of organic materials. To date, however, the limited number of fabrication techniques has forced a steep compromise between performance, reproducibility, range of feature sizes, gentle treatment of the single crystal, and facility of construction. Here we present a materials-general technique for the fabrication of single-crystal field-effect transistors with the use of a spin-coated elastomer gate dielectric and photolithographically defined source and drain electrodes. This allows the production of feature sizes and patterns previously impossible with reported elastomeric techniques, yet yields devices with performance far superior to those fabricated on nonconformal dielectrics.

Organic single-crystal field-effect transistors (SCFETs) have emerged as a workhorse for the exploration of transport phenomenon in organic materials, as well as for exploring the performance limit for available materials[1,2]. The long-range order inherent in the crystalline state allows the probing of properties *intrinsic* to molecular and solid-state structure. A number of techniques have been reported for the fabrication of SCFETs[3-8] in an effort to realize the combination of high performance, reproducibility, ease of production, and a wide range of feature sizes, while causing minimal damage to the fragile single crystal. The most successful efforts to this end have employed conformal elastomeric[4] and free-space[5] dielectrics, yielding the highest published mobilities for organic single-crystal transistors. It has been challenging, however, to achieve the above performance criteria while still allowing for feature sizes below hundreds of microns, limiting both the range of possible structures and the material candidates for single crystal studies. In this Letter, we present a materials-general method for the production of high-performance transistors with features as small as two microns, by defining electrodes photolithographically atop a spin-coated elastomer dielectric. This technique capitalizes on the advantages of elastomer dielectrics, as previously reported[4], but eliminates the need for manual transfer of the layer. In addition, spin-coating provides a flat, uniform surface compatible with photolithography, allowing feature sizes and device patterns not realizable with the transfer technique. We report excellent performance for rubrene, pentacene, and tetracene microscale transistors with channel lengths as small as two micrometers electrical characteristics reflecting the high quality of the semiconductor/dielectric interface.

As reported widely in literature, the chemical and morphological nature of the dielectric/active layer interface is absolutely critical to the performance of thin-film and single-crystal field-effect transistors. In particular, the oxide dielectric layer inherited from the silicon transistor has proven especially problematic, and has been held responsible for trapping, water formation[9], and the suppression of n-type behavior in otherwise ambipolar materials[10]. Even devices with relatively high performance have illustrated pronounced hysteresis and shift of threshold voltage with repeated and bidirectional testing[3]. In addition, trapping and slow turn-on may make calculated saturation-regime mobilities somewhat ambiguous and deceptively inflated. These problems have been circumvented primarily by depolarizing this interface, generally by treating the oxide surface with a non-polar monolayer such as octadecyltrichlorosilane (OTS). Another approach involves simply replacing the dielectric layer with a chemically inert and nonpolar layer, such as hydroxyl-free polymers[10] or an elastomer[4]. The method described here takes the latter approach, with the use of a non-polar elastomer dielectric layer, PDMS. While oxide device shows a pronounced hysteresis upon reverse of direction, characteristic of trapping at the oxide/crystal interface, the PDMS devices, show negligible hysteresis, demonstrating the quality, consistency, and inert nature of the interface.

Another key difficulty in the reproducible production of high quality single-crystal transistors is achieving consistently good contact between the semiconductor and both the source/drain contacts and the dielectric interface. In the bottom contact configuration – in which the electrodes are prefabricated on the substrate – the nearly perfectly flat crystal surface cannot touch the entire dielectric surface and the electrodes simultaneously. The alternative to this scheme – the top-contact configuration – requires electrode fabrication on top of the fragile crystal, possibly damaging it. The most successful compromises have been the conformal coating of parylene upon electrodes fabricated on the crystal surface[7], and the use of an elastomer[4] or air[5] dielectric in the bottom-contact configuration. These techniques each incorporate a conformal interface between the single crystal and both the dielectric and source/drain contacts, which results in a reproducible, high-quality contact.

In summary, we have presented a method for the reproducible fabrication of high-performance single-crystal FETs with a wide variety of feature sizes and with high density. This technique exploits a non-polar, chemically inert, and conformal dielectric layer to realize diminished contact resistance, negligible hysteresis and excellent electrical characteristics. With feature sizes limited only by lithography, this approach will allow the characterization of materials that produce crystals too small or fragile to be tested by current methods. The ease of fabrication and feature density of this structure will allow the detailed probing of material and device physics previously difficult to access with methods allowing only one device per crystal, such as contact resistance and the anisotropy of field-effect mobility.

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