Stability Analysis of Active Clock Deskewing Systems Using a Control Theoretic Approach

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Abstract—In this paper, a methodology for analyzing closed loop clock distribution and active deskewing networks is proposed. An active clock distribution and deskewing network is modelled as a closed loop feedback control system using state space equations. The state space models of the system were then used to simulate the clock deskewing scheme, and most importantly, to analyze the stability using the integral quadratic constraints method. Such a systematic analysis method can be very useful to designers as they will be able to determine how the deskewing network behaves, thus, avoiding repeated simulations. The proposed approach can be further extended to determine performance of such systems under different configurations. We show how the proposed method is applied to an experimental clock deskewing system for performance and stability analysis.

I. INTRODUCTION

Clock distribution has become an increasingly difficult task due to the current level of integration on VLSI chips and effects of process and environment variations on clock buffers and interconnects. Increasing clock rates places more stringent constraints on the maximum allowable skew and jitter for clock signals.

Existing clock distribution approaches can be broadly categorized into two different types of designs, namely, open loop and closed loop designs. The open loop design methods for clock distribution are based on implementing geometrically and electrically matched clock distribution structures to minimize skew on the chip. The most commonly used method for distributing clock signals in chips is to insert buffers either at the clock source and/or along a clock path, forming a *clock tree* structure. A mesh version of the clock tree structure is also used in which shunt paths further down the clock distribution network are placed to minimize the interconnect resistance within the clock tree. This mesh structure effectively places the branch resistances in parallel, minimizing the clock skew [1], [2], [3]. However, the mesh structure suffers from high power consumption. Another approach for distributing clock signals utilizes a hierarchy of planar symmetric H-tree or X-tree structures [1], [4], [2], [3]. Although, H-tree and X-tree structures consume less power, their ability to maintain less than 10% skew with increasing clock frequency becomes more and more challenging. Several attempts to introduce useful skew have been made [5] to utilize localized clock skew to improve synchronous performance by providing more time for the critical worst case data paths. However, useful skews are often determined at the design stage based on min and max data path delays, they cannot be used to account for process and environment variations. In order to compensate for skew in silicon, closed loop clock distribution systems known as the active deskewing systems, have been proposed by [6], [7], [8]. Clock deskewing systems exhibit disturbance rejection and are robust to modelling errors.

For a closed loop feedback system approach employed in an

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active deskewing scheme, stability is an important criterion. Existing analysis methods for the closed loop deskewing systems are based on repeated brute force simulations. These methods are very time consuming and do not give a definitive result by which one can say assertively that the system designed is stable or not. Since active deskewing systems employ closed loop techniques, it can be modelled as a closed loop control systems using control theory. Models for closed loop control systems can be easily analyzed for stability using existing control system theories. This paper presents a control theory formulation for active clock deskewing systems and a set of analysis methods for stability and performance analysis. We show that the proposed method can assert definitively whether a closed-loop clock deskewing system is stable. We apply the proposed method to an experimental deskewing system to illustrate the procedures of using the proposed method.

II. DESCRIPTION OF CLOCK DESKEWING SYSTEMS

In active clock deskewing systems, the entire chip is divided into many clock zones. Figure 1 shows the schematic of an example clock deskewing system [9].

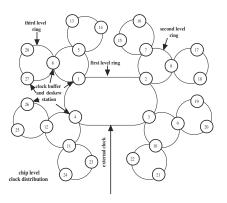


Fig. 1. Block diagram of 28 zone clock distribution network

The experimental clock deskewing system has 28 clock zones organized in a hierarchical ring structure. A topology with less number of hierarchies can also achieve deskewing, but with a different response characteristics. Clocks in each zone are derived from a clock buffer assigned to that zone. Clocks between different zones have a certain communication pattern to ensure that the skew across the chip is within a given specification. In the experimental clock deskewing system, the clock buffers in a each zone communicate with each other through a hierarchical ring structure as shown in figure 1. Each clock buffer adjusts its output based on the phase difference in the arrival time of the clock between it and its neighbors. When there is an exceeding amount of skew at a certain spot of the chip, clock buffers around the spot start to adjust their clock outputs to reduce the skew among the zones in and around the spot. Such adjustments may cause increase skew between clock zones around the spot and those further away from the spot. Hence a wave of adjustment is carried out throughout the chip until the skew is within the required specification.

The logical implementation of clock deskewing within a clock zone often involves comparators, programmable delay element and local clock distribution network with the clock zone. Figure 2 shows an implementation proposed for a 64-bit microprocessor design [8]. This design consists of a delay locked loop (DLL),

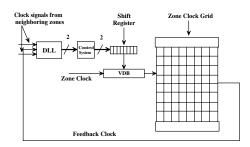


Fig. 2. Logical implementation of a deskew station

a control system, a shift register, a variable delay buffer (VDB), and a clock grid within the clock zone. The DLL compares the feedback clock signal from the zone clock grid with the clock signals from the neighboring zone clock grids. The DLL compares the clocks and generates a 2-bit signal which encodes the result of the comparisons. This signal is then sent to a control system which stores the results of previous N comparisons. The control system outputs a 1 or a 0 on its output depending on whether past N comparisons required to increment or decrement the delay to the zone clock. The shift register stores values of delays to be added through the VDB in the form of ones and zeros. If the comparisons for N consecutive clock cycles required the clock to be slowed down, the control system outputs a 1 on one of its bit lines which is then shifted into the shift register. The shift registers output is then set as inputs to the different programmable RC delay elements in the VDB once every clock cycle. This in turn increases the delay of the zone clock going to the various sequential elements in that zone connected by the zone clock grid.

At the chip level, the communication/compare pattern among clock zones can be determined based on floorplan and the deskewing requirements in terms of response time of the deskewing system and the amount of residue skews in the system. Figure 3 shows a 27-zone system with a slightly different communication/compare pattern at the chip level compared to that shown in figure 1. The goal of the 27-zone system is to improve response time at the expense of system complexity.

In summary, active clock deskewing systems often have the following characteristics:

- Active clock deskewing systems tries to minimize the overall skew through a distributed feedback control system.
- Each clock zone compares with a set of other clock zones to determine the amount the corrections needed in the zone.
- Useful skew can be incorporated into the deskewing system by presetting the default correction in each clock zone.
- Once the correction is done, the corrected clock signal in the clock zone is available at the beginning of the next clock cycle.

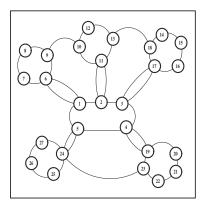


Fig. 3. Block diagram of 27 zone clock distribution network

- The amount of corrections in each zone is quantized to a set of steps. The size of the steps is determined by the response time requirement and the limitations of the delay adjustment circuits.
- To prevent increased clock jitter, each clock zone needs to receive a set of consistent correction signals in a set of consecutive clock cycles, and the adjustment to the clock is done only at a preset clock cycle intervals, such as every 10 clock cycles.
- To maintain a good center arrival time point for every clock zone on a chip, a global level adjustment pulling towards the center arrival time point is often needed.

III. SYSTEM MODELS AND STABILITY ANALYSIS USING CONTROL THEORY

The nature of the feedback clock deskewing system and the quantized adjustments to the clock phase fit well with nonlinear discrete time-invariant multiple-input/multiple-output (MIMO) control systems.

In general, the state space equation and the output equation of nonlinear continuous time-invariant MIMO control systems can be described as follows:

$$\dot{x}(t) = A(t) \cdot x(t) + B(t) \cdot I(t) \tag{1}$$

and

$$\dot{y}(t) = C(t) \cdot x(t) + D(t) \cdot I(t)$$
(2)

where x(t) is the present state vector of the system. y(t) is the output of this system and I(t) is a vector of inputs to this system.

The state space equation and the output equation for nonlinear discrete time-invariant MIMO systems can be shown as:

$$x_{k+1} = A \cdot x_k + B \cdot I_k \tag{3}$$

and

$$y_{k+1} = C \cdot x_k + D \cdot I_k \tag{4}$$

where x_k is the vector of current states of the system, x_{k+1} is a vector of next states. I_k is a vector of inputs to the system and y_{k+1} is the output of the system. The matrices A, and B in equations 1, and 3 describe the relationship between the inputs and current state to the next state of the system. Matrices C and D in equations 2, and 4 describe the relationship between inputs and current state to the outputs of the system. The matrix A is also often referred to as the system matrix. With corrections through the feedback structure in the clock deskewing systems, the state space equation can be written as:

$$Tarr_{k+1} = T_{nom} + Tarr_k + U \cdot Tarr_k$$
(5)

where T_{nom} is nominal clock period of the system. $Tarr_{k+1}$ is a vector describing the arrival times of the clock in all the clock zones in the next clock cycle and $Tarr_k$ is a vector describing the arrival times of clock in all the clock zones in the current clock cycle. The matrix U describes the connections in the clock feedback/correction scheme along with the gains that are associated with the different zone comparisons. $U \cdot Tarr_k$ represents the amount of correction, ΔT_r , each clock zone should get in the next clock cycle.

Let's take a simple 4-zone system, shown in figure 4, as an example. The amount of correction, ΔT_r , at each zone comes

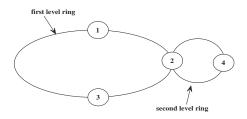


Fig. 4. A simple active deskewing network with 4 clock zones

from comparing its neighboring zones as specified in the topology. Based on the connections shown in figure 4, the amount of correction at each zone can be expressed as:

$$\Delta x 1_{k+1} = k [x 3_k - x 1_k]$$

$$\Delta x 2_{k+1} = k [(x 1_k - x 2_k) + (x 4_k - x 2_k)]$$

$$\Delta x 3_{k+1} = k [x 2_k - x 3_k]$$

$$\Delta x 4_{k+1} = k [x 4_k - x 4_k]$$
(6)

where $k_i \neq 0$ represents connections between the clock zones and the gain of skew adjustment. The correcting term for zone 1 is proportional to the skew between zone 1 and zone 3 as illustrated in figure 4. The U matrix of the 4-zone system can be represented as:

 $\Delta X_{k+1} = UX_k$

and

$$U = \begin{bmatrix} -k_1 & 0 & k_1 & 0 \\ k_2 & -2 \cdot k_2 & 0 & k_2 \\ 0 & k_3 & -k_3 & 0 \\ 0 & k_4 & 0 & -k_4 \end{bmatrix}$$
(8)

For a given feedback pattern, the deskewing pattern of the system is defined, and therefore, the matrix U can be uniquely defined.

When correcting the clock arrival time for a given zone based on skew, the amount of correction is often discrete due to quantized increments and decrements of delay. To account for quantized adjustments, we define *step* as the minimum amount of delay by which the variable delay buffer (VDB) increases or decreases the arrival time of the clock at each clock zone. In addition, adjustments to the clock arrival time of a clock zone should be made based on "real" skew between clock zones, rather than false skew caused by potential jitter. Therefore, adjustments to the clock arrival time of a clock zone will be made if there are consecutive skew comparison results of the same direction between two clock zones. To simplify the discussion without losing generality, we assume that the window for preventing clock jitter is 3 clock cycles. That is: a clock zone in the deskewing system needs to wait for consistent "increase" or "decrease" requests from its neighbors in 3 consecutive clock cycles before it will adjust its own clock output. The corrections to a clock zone can be written as:

$$\Delta Tr_1 = f(mod(clk_cycle, n) \cdot step \cdot f(\frac{1}{3}(sign[U \cdot Tarr1_k] + sign[U \cdot Tarr2_k] + sign[U \cdot Tarr2_k]))$$
(9)

where $Tarr1_k$ is the current state vector containing the arrival time of the clock in each zone of the deskewing system at the k^{th} instant. $Tarr2_k$ is the state vector containing the arrival time of the clock in each zone of the distribution at the $(k-1)^{th}$ instant. $Tarr3_k$ is the state vector containing the arrival time of the clock in each zone of the distribution at the $(k-2)^{th}$ instant. These past values of arrival times are used so as to make a correction only if the same type of correction (either positive or negative) was requested in the previous two consecutive clock cycles as well. For example, consider the case when the previous two comparisons of clock arrival times for any zone required the zone to speed up the clock arrival time for that zone. If the current comparison also requires the clock arrival time to speed up, only then will the clock arrival time for that zone be sped up. The function f in equation (9) is a threshold function and can be defined as:

$$f(x) = 1, x \ge 1$$

= 0, -1 > x < 1
= -1, x \le -1 (10)

The term $f(\frac{1}{3}(sign[U \cdot Tarr1_k] + sign[U \cdot Tarr2_k] + sign[U \cdot Tarr3_k]))$ checks if the values of the past two comparisons were the same as the result of the current comparison. It outputs a 1 or a -1 depending on whether three consecutive comparisons required the delay to be increased or decreased by a step size, and 0 otherwise.

The function, *mod*(*clk_cycle*, *n*), in equation 9 allows the adjustments to the clock arrival time of clock zones n-1 clock cycles out of every n clock cycles. The one remaining clock cycle in every n clock cycles are used for the global clock arrival time adjustment to accommodate the centering of arrival time. This may be desirable to ensure that there is no systematic drift of clock arrival time at the global level. Such a scheme can be modeled as:

$$\Delta Tr_2 = 5 \cdot step \cdot [1 - f(mod(clk_cycle, n))] \cdot f(period \cdot k - Tarr1_k)$$
(11)

Equation 11 describes a mechanism that speeds up or slows down the clock in each zone once in every n clock cycles by five times the nominal step size where $period \cdot k$ represents the nominal clock arrival time at time k. The nonlinear model to describe the active deskewing system can be formulated as:

$$Tarr1_{k+1} = Tarr1_k + \Delta Tr_1 + \Delta Tr_2 \tag{12}$$

Using the simple 4-zone example in Figure 4, and assuming that step size is 5 ps, and the initial arrival times of all clock zones except zone 2 be zero. We introduce a disturbance of 20 ps in the arrival time of the clock at zone 2. The matrices $Tarr1_1$, $Tarr2_1$, $Tarr3_1$, and *period* are:

$$Tarr1_k = \begin{bmatrix} 0\\ 20\\ 0\\ 0\\ 0 \end{bmatrix}$$
(13)

(7)

$$Tarr2_k = \begin{bmatrix} 0\\0\\0\\0 \end{bmatrix}$$
(14)

$$Tarr3_k = \begin{vmatrix} 0\\0\\0\\0\end{vmatrix}$$
(15)

$$period = \begin{bmatrix} 350\\ 350\\ 350\\ 350\\ 350 \end{bmatrix}$$
(16)

The matrix U has been expressed in equation . Assuming $k_i = 1$ and plugging in the above values in equation 12, the arrival times of clock in the four zones are calculated. Table II below shows the skew between the clock arrival times of all the four zones which are calculated from the arrival times of clock for each zone, shown in Table I.

 TABLE I

 Arrival times of all the clock zones for 8 clock cycles

 Using the nonlinear model.

Clock cycle	1	2	3	4	5	6	7	8
Zone 1	0	350	700	1050	1400	1750	2105	2460
Zone 2	20	370	720	1065	1410	1755	2105	2455
Zone 3	0	350	700	1055	1410	1760	2110	2460
Zone 4	0	350	700	1055	1410	1760	2110	2460

TABLE II Skew of the clock zones for 8 clock cycles calculated from Table I.

Clock cycle	1	2	3	4	5	6	7	8
Zone 1	0	0	0	-5	-10	-10	-5	0
Zone 2	20	20	20	-10	-10	-10	-5	-5
Zone 3	-20	-20	-20	-10	0	-5	5	5
Zone 4	-20	-20	-20	-10	0	-5	0	0

A. Stability Analysis of Nonlinear Model

It is clear from the discussions in the previous sections that the clock deskewing system can be modelled as a nonlinear MIMO system. One of the most fundamental questions concerning the clock deskewing systems with distributed feedback control loop shown in Figures 1 and 3 is that of stability. Is the system stable irrespective of the jitter/skew perturbation, that is, do the system eventually settle to desired states after perturbations have occurred? A brute force approach to answer this question is Monte-Carlo type simulations. But this approach is very expensive. Analytically proving stability of a nonlinear time-invariant system is very difficult in general. However, if the nonlinearity of the system fits into a certain set of special cases, a variety of methods can be used for stability analysis [10],[11],[12]. One of the unifying methods for nonlinear control system stability analysis is integral quadratic constraints (IPC) [13],[14],[15],[16],[17]. In the IQC framework, the nonlinear functions can be bounded using sector-bounded limiting nonlinearity. In other words, the nonlinear functions in a system are replaced by linear functions that are upper bound of the nonlinear functions. We then prove whether the control system with the linear upper-bound functions is stable

under any circumstances. Stability analysis for linear systems is well established and understood. If the sector-bound linear system is proven to be stable, the nonlinear system must also be stable. However, if the sector-bound linear system can not be proven to be stable, the stability of the nonlinear system is unknown.

In the system model in equation 12, the nonlinear functions mod, sign, and the threshold function f are bounded using linear functions. One of the sector blocks (sector-bound linear functions) used in the IQC analysis toolbox [16] is shown in figure 5. For example, the nonlinear element f in equation 12 can be

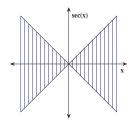


Fig. 5. Sector block in IQC toolbox

approximated using a modified sector block:

$$\frac{1}{2} + \frac{1}{2} \cdot \sec \tag{17}$$

This modified sector block is shown in figure 6. The function f

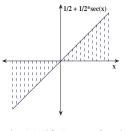


Fig. 6. Modified sector function

can be approximated using the modified sector block as shown in figure 7. The nonlinear element $f(mod(clk_cycle, 10))$ can be

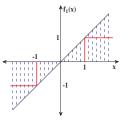


Fig. 7. Approximation of element f using the modified sector block

approximated using the modified sector in equation 17 as shown in figure 8. Approximation of $[1 - f(mod(clk_cycle, 10))]$ is shown in figure 9.

Using these modified sector blocks, the entire nonlinear system model can be built in *SIMULINK* using the IQC toolbox. Equation 18 describes the nonlinear model after replacing the nonlinear

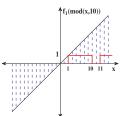


Fig. 8. Approximation of element $f(mod(clk_cycle, 10))$ using the modified sector block

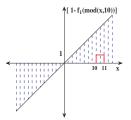


Fig. 9. Approximation of element $[1 - f(mod(clk_cycle, 10))]$ using the modified sector block

elements in equation 12 with sector blocks from the IQC toolbox.

$$Tarr1_{k+1} = T_{nom} + Tarr1_k + \left(\frac{1}{2} + \frac{1}{2} \cdot \sec\right) \cdot step \cdot \left(\frac{1}{2} + \frac{1}{2} \cdot \sec\right) \cdot \left(U \cdot Tarr1_k\right) + \left(\frac{1}{2} + \frac{1}{2} \cdot \sec\right) \cdot \left(U \cdot Tarr2_k\right) + \left(\frac{1}{2} + \frac{1}{2} \cdot \sec\right) \cdot \left(U \cdot Tarr3_k\right)\right) + 5 \cdot step \cdot \frac{1}{2} + \frac{1}{2} \cdot \sec \cdot \frac{1}{2} + \left(\frac{1}{2} \cdot \sec\right) - states1_k\right)$$
(18)

To help illustrate the modeling of the proposed non-linear deskewing system, Figure 10 shows the various blocks present in the IQC toolbox that were used to build the simulink model of the nonlinear system. The *SIMULINK* block diagram of the 27-zone nonlinear active deskewing system for analysis of stability using IQC toolbox is shown in figure 11.

IV. EXPERIMENTAL RESULTS

A. Model Simulations and Verification

Results of simulations for the nonlinear models are shown in this section. All simulations were performed for a duration of 300 clock cycles. External noise in the form of clock jitter was introduced to all test systems at clock cycles 10, 60, 110, 160,

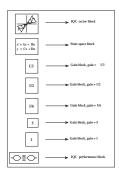


Fig. 10. Blocks used in IQC toolbox

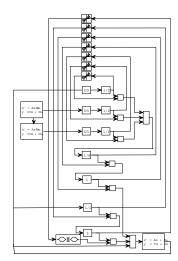


Fig. 11. Block Diagram of the Nonlinear Model using IQC toolbox

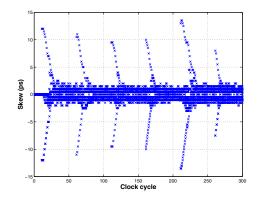


Fig. 12. Clock skew of each zone for the nonlinear 28-zone clock distribution system

210, and 260. Figure 12 shows the skew of each of the zones in the 28-zone system and figure 13 shows the skew of each of the zones in the 27-zone system. It can be seen from Figures 12 and 13 that there is no skew disturbances until the 9th clock cycle. In the 10th clock cycle, an external disturbance in the magnitude of 12 ps was applied to the system, and we observed skew of ± 12 ps. The system response was to deskew the external clock disturbance which was introduced in the 10th clock cycle. Both systems deskewed the external jitter 20 clock cycles after its occurrence, which is the acquisition time of the system. However, as seen from Figure 12 the residual skew present in the 28-zone system after the deskewing operation is approximately 2 ps, whereas the residual skew present in the 27-zone system is approximately 1 ps as shown Figure 13. The amount of residual skew present in the system after the deskewing operation complete determines the resolution of the deskewing system. Hence the 27-zone system exhibits better resolution and hence better noise rejection properties as compared to the 28-zone system. However, the 27-zone system is more complex and requires more connections and comparisons among different clock zones. The requirement for the amount of residue skew in the clock system will determine the topology and the complexity of the deskewing system.

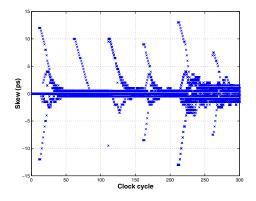


Fig. 13. Clock skew of each zone for the nonlinear 27-zone clock distribution system

B. Results for Nonlinear Model Stability Analysis

Stability analysis of the nonlinear model was performed by implementing the modified nonlinear model in equation 18 where the nonlinear elements were replaced using the sector blocks. The delay blocks were created using state space models since the IQC toolbox does not contain discrete delay elements in the *iqc_lib SIMULINK* library. The performance block was used to analyze the stability of this nonlinear system. The performance block is required to be used by the *iqc_gui* command in order to determine if the system is stable or not. The *iqc_gui* command when used to determine stability of systems, returns an output value of *iqc_gain* if the system is stable else it does not return any value for *iqc_gain*. Step size for the deskewing system was set to 0.5 ps.

C. Unstable Nonlinear System Example

It is possible that the entire deskewing system becomes unstable. This happens when the clock zones keep over-compensating for the skew. Stability is guaranteed only for a certain range of step size by which the adjustment to the arrival time of the clocks are adjusted. The range for values of step in equation 18 depends on the topology of clock distribution network. It also depends on how often the adjustments need to be done on the clock arrival times. For the 4-zone system shown in figure 4, the value of step for which the system became unstable was found to be 9 ps. The simulation results for the 4-zone system using the nonlinear model in equation 18 is shown in figure 14. As seen in the results, the skew of each zone in the systems keeps increasing since the system overcompensated for the skew, thus making the system unstable. This result is also confirmed by using IQC stability analysis.

In general, it is relatively easier for Monte Carlo simulations to detect an unstable system. However, it is not possible for Monte Carlo simulations to prove a system in stable. The confidence grows with increasing amount of simulations. The proposed approach using control theory can prove a system is stable a much less amount of effort.

Simulations for stability analysis for the nonlinear systems were performed using the IQC-toolbox for Matlab. The CPU time for stability analysis for the 28-zone and 27-zone systems were 350 and 276 minutes, respectively, running on a 1.9GHz Pentium4 processor with 512MB of memory.

V. CONCLUSIONS

This paper presents a systematic approach using control theory to design and verify the stability of active clock deskewing

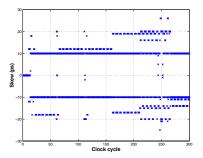


Fig. 14. Clock skew for each zone in an unstable 4-zone system

systems. Current methods of brute-force simulations to verify the stability of the closed-loop active-deskewing systems are slow and incomplete. By modeling the active clock deskewing systems as closed loop nonlinear feedback control systems and analyzed them using IQC theory to determine stability, the proposed method has the benefits of much faster analysis speed and much higher confidence of the results. The use of the proposed method is demonstrated using a 27-zone and a 28-zone clock deskewing system with successful verification of their stabilities.

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