A High-Speed Externally Compensated Operational Amplifier

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***Abstract*—This paper describes the design of a high speed externally compensated operational amplifier and its advantages and disadvantages over their internally compensated counterparts.**

I. Introduction

An externally compensated operational amplifier is an op amp that allows the user to tailor its open-loop transfer characteristics by means of an external network. There are two classes of externally compensated op amps, single-stage and two-stage. Single-stage types have a single gain stage and therefore have one high-impedance node to which a passive network can be connected to define their open-loop transfer function. In these units, the compensation network is connected from the high-impedance node to signal ground. Figure 1 shows a simplified diagram of a single-stage op amp where a single capacitor has been used as a compensation network to implement a dominant-pole transfer function (a -20dB roll off over a wide frequency range).

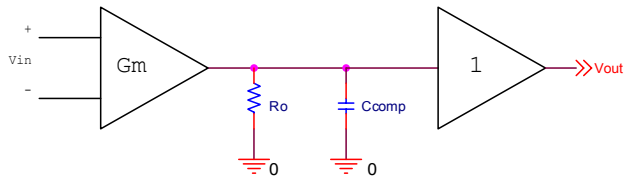

Fig. 1. Simplified diagram of a single-stage externally compensated operational amplifier with capacitive dominant pole compensation.

Two-stage externally compensated operational amplifiers are composed of two gain stages and thus they possess two high-impedance nodes. The compensation network is connected between these two nodes forming a minor feedback loop within the op amp. Figure 2 shows a simplified diagram of a two-stage externally compensated op amp with the compensation network around the second gain stage. In the case where a single capacitor is used as a compensation network, these op amps are known as Miller multiplied or Miller compensated operational amplifiers. This name is a misleading since the Miller effect is caused by minor loop feedback. Figure 3 shows the block diagram of the compensated operational amplifier depicting the minor loop within the amp. This loop feeds back a current proportional to the admittance of the compensation network and the op amp's output voltage to the input of the second stage. Feedforward effects through the compensation network have not been included on the diagram; it will be argued later why this is the case. Since this op amp has a high gain in the forward path of the minor loop, the open-loop transfer characteristic is set by the compensation network over a wide frequency range.

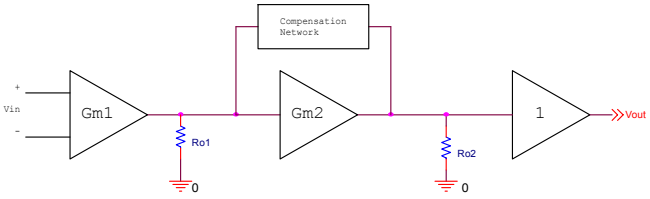

Fig. 2. Simplified diagram of a two-stage externally compensated operational amplifier with a generic compensation network.

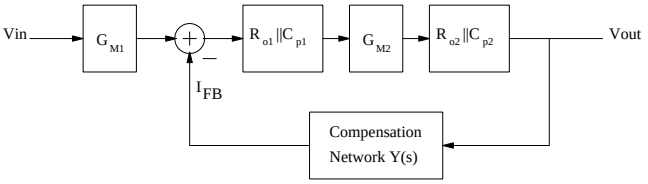

Fig. 3. Block diagram of a two-stage externally compensated operational amplifier showing the minor loop formed by the external compensation network.

The presented op amp belongs to the second class and it presents several advantages over single-stage and internally compensated units. In order to achieve good stability over a large range of closed-loop gains, internally compensated op amps use a dominant pole compensation scheme and as a result suffer from constant gain-bandwidth product, which reduces the closed-loop bandwidth as the closed-loop gain

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increases. Also, these amps have trouble driving heavy capacitive loads since the loading capacitor forms a pole with the output impedance. This pole appears in the major loop of the op amp and can cause stability problems. Finally, the user of these units is stuck with the dynamics offered by a single pole roll-off transfer function, in the sense that it will only provide zero steady-state error to a step input but not to a ramp.

Single-stage externally compensated operational amplifiers are more flexible than internally compensated units because they do not suffer from constant gain-bandwidth product limitations. If the op amp is configured to provide certain gain, the compensation network can be chosen to optimize the bandwidth at that gain. Also, they allow the introduction of zeros in their major loop transfer function (using a series RC compensation network) such that the op amp can drive heavy capacitive loads. However, one problem with these amps though is that a roll-off slope steeper than -20dB per decade in the open-loop transfer function is not possible because the compensation network is connected to signal ground. Thus, compensation schemes like two-pole compensation are unachievable.

Two-stage externally compensated op amps can implement almost any open-loop transfer function. Thus, they can be compensated to excel in performance under any conditions. This flexibility is due to the minor loop in their architecture where the open-loop transfer function of the op amp will follow the inverse of the transfer function of the minor loop's feedback path (1/Y(s) in figure 3) as long as the minor loop's loop-gain is greater than one. The major disadvantage of these op amps is that since they posses an inner loop, the user has to make sure that both major and minor loop are stable when the op amp is connected in a feedback configuration.

II. Problems At Large

Although externally compensated op amps have plenty of advantages to offer, they have two inherent problems that limit their performance. The first one has to do with the availability of passive components used in the compensation network. For example, for a two-stage operational amplifier, such as shown in figure 2, with an input-stage transconductance (G_{M1}) of one millimho, to achieve a unity-gain (A_{CL}=1) bandwidth of 150MHz ($2\pi\omega_c$), equation one states that the optimum compensation capacitor would be 1pF (assuming capacitive dominant pole compensation is used).

$$C_c = \frac{Gm_1}{A_{CL}\, 2\pi \cdot \omega_c} \qquad (1)$$

If a closed-loop gain of ten (A_{CL}=10) is desired, the optimum compensation would be achieved using a 0.1 picofarad capacitor (equation one determines C_c such that the closed-loop bandwidth of the op amp is kept constant, thus the gain-bandwidth product is increased as A_{CL} increases). As the desired closed-loop gain-bandwidth product increases, the size of the passive components that form the compensation network shrink drastically. This is a big problem, since in today's market, good small-sized passive components may not only be hard to find, but can be very expensive (even more than the op amp itself).

The second problem has to do with the parasitics encountered when taking critical parts of an integrated circuit off-chip, in our case the compensation network. These parasitics include the capacitance of the bond pads and the inductance of the bond wires (these connect the die to the package leads), the self and mutual inductance of the leads, the capacitance between the leads, the transmission line effects of the PCB board traces and capacitance of the soldering pads. All of these appear in the compensation path and as a result affect the behavior of the op amp. A typical value for the sum of all these parasitics is about 0.5pF of capacitance and about 5nH of inductance. From our discussion above we can see that their size is quite comparable to the components used in the external compensation network.

These two problems are addressed by the proposed amplifier as described in the next section.

III. The Proposed Amplifier

As mentioned in section I, the presented operational amplifier belongs to the two-stage externally compensated class. The amplifier possesses two gain stages, each composed of a transconductor cell (G_M) and an output resistance (R_O). G_{M1} denotes to the transconductance of the first stage and G_{M2} to the transconductance of the second stage. Accordingly, R_{O1} denotes the overall resistance at the output node of the first stage and R_{O2} the overall resistance at the output of the second stage. The amplifier includes a voltage buffer between the two gain stages and between the second stage and output of the circuit. The first one is included to prevent inter-stage loading effects while the second reduces the open-loop output resistance of the overall amplifier and enhances its output current handling. Finally, an interface circuit has been included between the second compensation terminal and the output of the first stage. The detailed model of the amplifier is shown in figure 4.

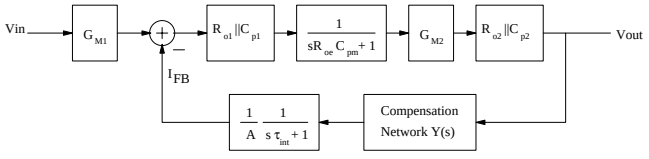

Fig. 4. Block diagram for the proposed operational amplifier.

The structure shown in the model for the proposed of op amp is quite standard with the exception of the interface circuit block. The main purpose of this interface is to reduce the effects of parasitics in the compensation network and to enable the user to use reasonably sized components. The two main problems of externally compensated amplifiers are addressed by using an 'enlarged' external compensation network (bigger admittance) and making it look 'small' to the operational amplifier by attenuating the current signal fed back by the compensation network by means of the interface block as shown in figure 4.

The inclusion of the interface moves the limits in performance of the op amp from the available external network components and surrounding parasitics to the achievable performance of the interface. The interface circuit is included within the minor loop of the amp and any singularities it introduces (poles and zeros) will affect the behavior of this loop. As the model shows, the interface has a finite bandwidth which introduces a pole within the loop. The circuit also has finite input impedance which will create a pole with any capacitance attached to the interface input. These two poles severely degrade the stability of the minor loop and can drive it to instability. The figures of merit of the interface will dictate the overall performance of the amp. A more detailed analysis is performed in section V.

The presented model neglects any feed-forward effects (from the output of the input stage to the output of the second stage) via the compensation network. This is due to the fact that the interface circuit is unilateral and thus it blocks any signals from traveling in the feed forward direction (i.e. from the output of the input stage to the output of the second stage). As a result, unwanted effects like the right half plane zero in purely capacitive Miller compensation are avoided.

Although the model in figure 4 describes the presented amplifier in detail, it has a few shortcomings. First, it does not show large signal currents. Since the current signal injected into the output of the first stage (I_{FB}) is attenuated by the interface to allow the admittance of the compensation network to be enlarged (bigger compensation capacitor in the case of purely capacitive compensation), the current that has to be provided by the second stage is vastly increased. For example, a 10pF compensation capacitor with the attenuation of ten in the interface creates an effective capacitance of 1pF. If the input stage outputs 100uA of current into the 'effective compensation capacitor' the op amp's output will rise at rate of 100V/us (SR=I/C). To accomplish this, the second stage has to provide 1mA, ten times more current due to the interface's attenuation. This problem arises from the fact that the admittance of the compensation network is reduced only on one side, i.e. to the output of the input stage but not to the output of the second stage. As shown in section IV, to overcome this problem, a current on demand second stage is used.

Also, the model does not show how the forward path of the op amp is affected by the compensation network. In the input stage, this shortcoming can be neglected since the output capacitance of the interface is quite low (less than 0.1pF) and output impedance of the interface is quite high. On the other hand, since the compensation network is connected directly from the output of the second stage to virtual ground (input of the interface), the second stage is considerably loaded. This loading is particular to the compensation network in use and this effect has to be taken into consideration when compensating the amplifier.

Figure 5 shows a simplified circuit diagram of the proposed op amp illustrating the components shown in the model. Figure 6 shows a simplified circuit schematic of the interface.

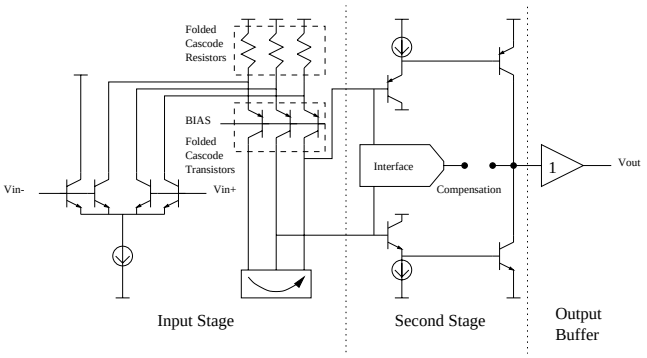

Fig. 5. Simplified schematic of proposed op-amp.

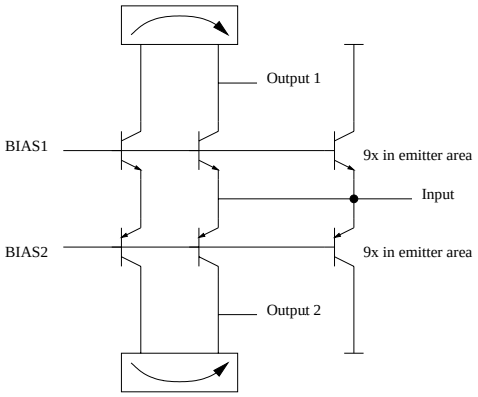

Fig. 6. Simplified schematic of interface circuit.

IV. Description Of The Circuit

A. The Input Stage

The input stage uses a special folded cascoded topology as shown in figure 5, which allows the biasing of the second stage. The cell is made up of a degenerated differential pair which serves the purpose of a transconductor and thus gives the G_{M1} block. The current signal generated by the differential pair is then conveyed by the folded cascode transistors to the outputs of the input stage. At the point

where the current signal is folded, there is some current signal loss due to the folded cascode resistors which shunt some of the signal and return it to the positive supply. This causes an effective input transconductance reduction.

The input stage provides two high-impedance outputs which drive the top and bottom halves of the second stage. This drive method addresses the increased large signal current requirement imposed on the second stage.

Finally, although there are two input stage outputs, this is transparent to the user of the op amp since the interface splits evenly the current from the compensation network and injects each half to each output.

B. The Second Stage

The second gain stage uses a complementary Darlington arrangement which includes a cascade of an emitter follower buffer and a common emitter gain stage as shown in figure 7. The circuit is 'top to bottom' symmetric in the sense that it has the same configuration sharing the same output node while each half is driven from one of the outputs of the input stage. The top half of the circuit is referred to the positive supply, while the bottom half is referred to the negative supply. Since Darlington configurations can only provide unlimited current in one direction, by using this symmetric arrangement, the problem of supplying augmented large signal currents due to the interface's current division is solved.

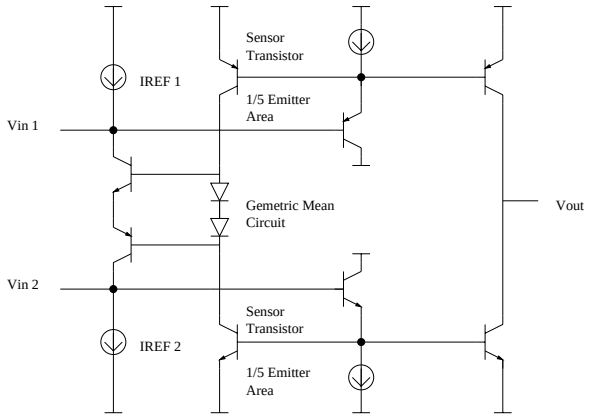

Fig. 7. The second stage.

C. The Output Stage

The output stage is a complementary emitter follower which provides a low open-loop output impedance and high current drive to the amplifier such that the circuit can handle a wide range of resistive and capacitive loads.

D. The Interface

The purpose of the interface is to is to attenuate the current injected by the compensation network into the input stage's output, such that the admittance of the compensation network looks reduced to the op amp, and thus enlarged components, which are readily available, can be used. As a result, the parasitics associated with the bonding wires, bonding pads and pc-board traces are shadowed.

The circuit uses two complementary current buffers with their inputs connected together and their bias currents set in a 9:1 ratio. Therefore, their input impedances are also in a 9:1 ratio which forces the current going into the interface to divide between them in a 9:1 ratio. Thus, by feeding back the current from the buffer that captured a tenth of the input current, the attenuation functionality is achieved.

Complementary buffers are used in order to allow a wide range of input currents (positive and negative), since in theory this topology can sink and source unlimited current. In reality, parasitic resistances limit the maximum input current the circuit can handle, but in practice these bounds are much higher than any reasonable input current the interface might have to face.

V. DYNAMICS

The performance limits of the operational amplifier have been moved from the availability of external components and the presence of trace, pin and pad parasitics to the achievable performance of the interface. The interface has a bandwidth of f = 2GHz, such that at this frequency, the magnitude of current signal injected to the output of the input stage starts to roll off at -20dB/dec. As a consequence, the compensation feedback path shown in figure 4 becomes ineffective and the amplifier does not follow the behavior expected from the compensation network being used. In practice, the roll-off seen at frequency f in the magnitude of the interface's current gain is an steeper than -20dB/dec since the bandwidth of the interface is around f_T of the transistors which implies that multiple poles are expected at frequency f.

Also, the interface has finite input impedance that appears in series with the compensation network and thus it will create a pole with any capacitance at the input of the interface. If the current gain of the interface was one, a short circuit has been replaced with a limited bandwidth resistive short circuit

A more quantitative analysis can be done using the model shown in figure 4. Given that there are many possibilities for the admittances that can used in the compensation block, it is impossible to model them all. It is a good assumption that when the amplifier is compensated, the magnitude of its open-loop gain (A_{OL}) must cross over with a -20dB/dec roll off. Stability can also be guaranteed with a crossover of -40dB/dec if the crossover frequency is surrounded by sections of -20dB/dec roll-off. This case will be ignored since it is not usual is op amp compensations. Simple capacitive compensation, which provides a -20dB/dec roll-off over a wide frequency range, can be used to model the high frequency behavior of many compensation

networks.

Using a single capacitor (C_C) as the compensation block, the block admittance becomes

$$Y(s) = \frac{1}{sC_C}. \tag{2}$$

This compensation choice alters the model in figure 4 since it increases the capacitive load at the output of the second stage because it appears in parallel with C_{P2}. Also, capacitor C_C forms a pole with the input impedance of the interface, thus it adds a singularity to the amplifier's minor loop feedback path. The loop transmission of the op-amp's minor loop is given by

$$L_m(s) = G(s) \cdot H(s) \tag{3}$$

where G(s) is the forward path of the minor loop,

$$G(s) = G_{M1}\left(\frac{R_{O1}}{R_{O1}C_{P1}s+1}\right)G_{M2}\left(\frac{R_{O2}}{R_{O2}(C_{P1}+C_C)s+1}\right) \tag{4}$$

and H(s) is the feedback path of the minor loop,

$$H(s) = \frac{1}{G_{M1}} \cdot \frac{1}{A} \cdot \frac{1}{\tau_{INT}s+1} \cdot \frac{1}{sR_{IN}C_C+1} \cdot sC_C. \tag{5}$$

R_{IN} is the input resistance of the interface, τ_{INT} is the time constant associated with the bandwidth of the interface and A is the DC current gain of the interface. Equations (3) through (5) show how the limitations of the interface appear as poles in $L_m(s)$ and damage the stability of the minor loop. The pole associated with the inter-stage buffer has been omitted since it is at a very high frequency and its effects are negligible.

In order to obtain the open-loop transfer function of the amplifier, A_{OL}, Black's formula can be applied such that,

$$A_{OL} = \frac{G(s)}{1+L(S)} = \frac{G(s)}{1+G(s)H(s)} = \frac{G(s)/H(s)}{1/H(s)+G(s)}. \tag{6}$$

If G(s) >> 1/H(s), then $A_{OL} \approx$ 1/H(s), and if G(s) << 1/H(s), then $A_{OL} \approx$ G(s). If G(s) and 1/H(s) are plotted on the same Bode plot, then A_{OL} can be approximated as the lower curve of the two.

Figures 10 through 17 show the Bode plot of the open-loop gain A_{OL} for some possible compensation schemes that could be used in the presented operational amplifier. Also, the step responses for these compensation schemes are shown.

In figure 10, purely capacitive compensation has been used with three compensation capacitor sizes: 10pF, 1pF and 0pF. Using this scheme, the operational amplifier's bandwidth can be optimized for closed-loop gains of 1, 10 and 100. From the plot, the bandwidths for these closed loop gains are 163MHz, 119MHz and 50MHz respectively with phase margins of 66°, 54° and 61°. Figure 11, shows the step response for these three closed loop gains. The rise time for the closed loop gain of 100 configuration (circles) is significantly lower than for the other closed loop gains. This is because the bandwidth for this configuration is limited by an internal parasitic capacitance that shows up in parallel to the interface. Also, since this parasitic capacitance by-passes the interface and the compensation capacitor used for this configuration is zero, the stability of the amplifier is better for a closed loop gain of 100 than for a closed loop gain of 10 (boxes) due to the interface not being on the signal path.

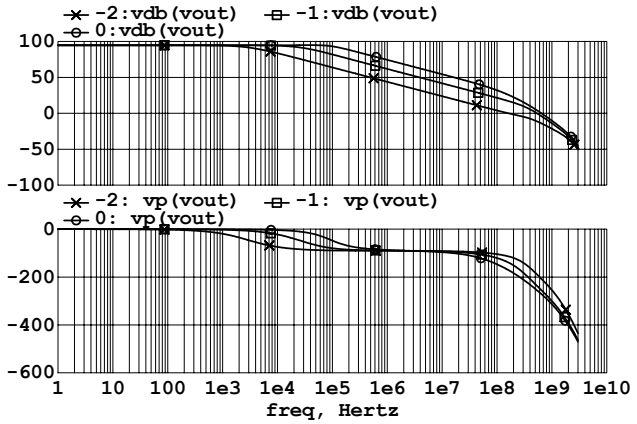

Fig. 10. Open-loop gain Bode plot for capacitive compensation using 10pF, 1pF and 0pF.

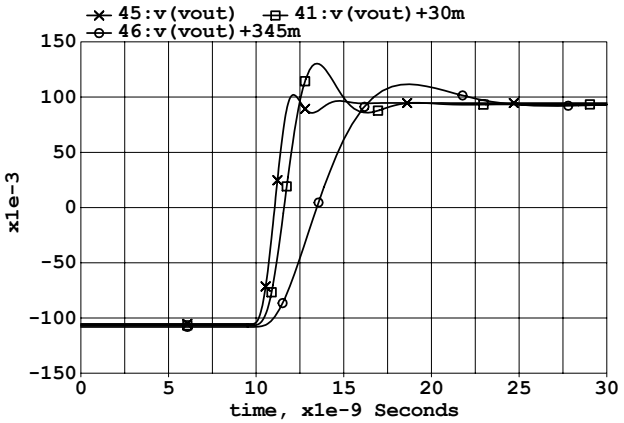

Fig. 11. Step response for capacitive compensation with closed loop gains of 1 (crosses), 10 (boxes) and 100 (circles) with respective compensation capacitors 10pF, 1pF and 0pF.

Figure 12 shows the open-loop gain of the amplifier when a series RC compensation network is employed. This scheme introduces a zero in the open-loop gain transfer function allowing the operational amplifier to drive heavy capacitive loads. A large capacitor at the output of the op-amp forms a pole with the op-amps output impedance, and this pole appears in open-loop gain transfer function.

The zero introduced by the RC network should cancel out the detrimental effect caused by the load capacitance pole.

Figure 13 shows the Bode plot of the op amp's open loop gain when it is compensated as in figure 12 but with a 50nF load capacitance. The unity gain bandwidth is about 29MHz with a phase margin of 53°. The step response for a closed loop gain of one is shown on figure 14.

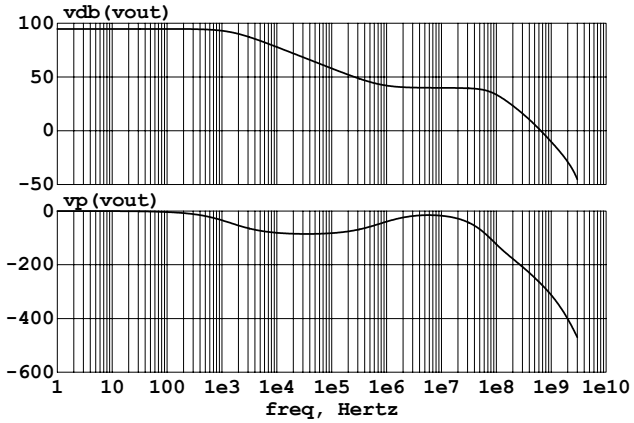

Fig. 12. Open-loop gain Bode plot for a series RC compensation scheme.

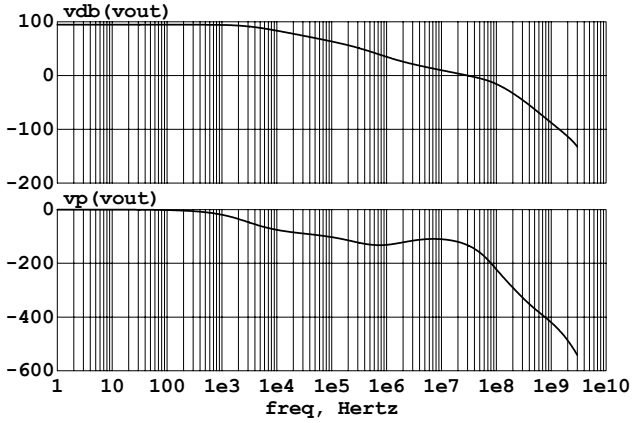

Fig. 13. Open-loop gain Bode plot for a series RC compensation scheme with CL=50nF.

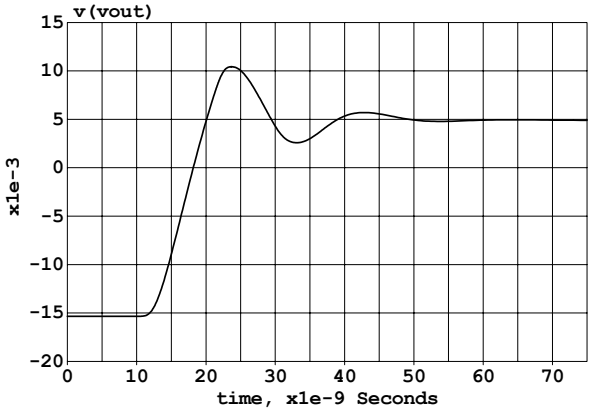

Fig. 14. Step response for RC compensation with a 50nF load capacitor.

Figure 15 shows the open-loop gain of the amplifier when two-pole compensation is employed. This scheme allows the amplifier to have zero steady state error to a ramp input.

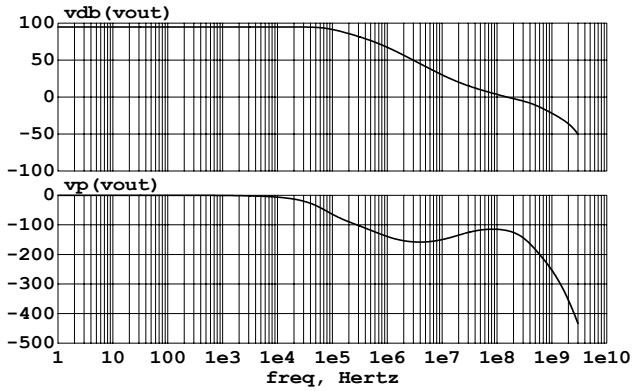

Fig. 15. Open-loop gain bode plot for a two pole compensation scheme.

Figure 16 shows the error signal to an input ramp using single-pole and two-pole compensation. The two-pole compensation scheme vastly reduces the steady state error.

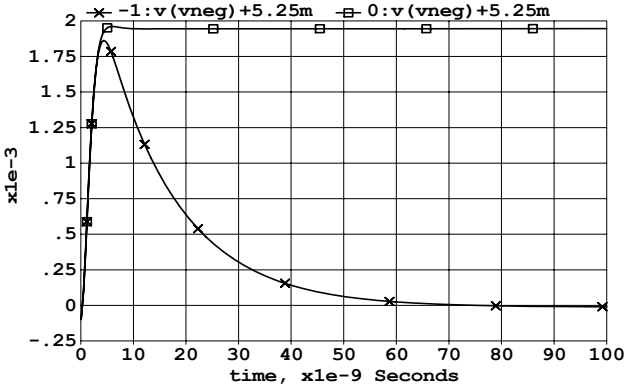

Fig. 16. Error signal to an input ramp using for two-pole (crosses) and single-pole (boxes) compensation.

VI. CONCLUSION

An externally compensated operational amplifier design has been presented. The amplifier includes a novel interface circuit which moves the limitations in performance from compensation components availability and board parasitics to the performance of the interface itself.

ACKNOWLEDGMENT

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REFERENCES

[1] Solomon, James E. "The monolithic op amp: a tutorial study," *IEEE Journal of Solid-State Circuits,* vol. SC-9, No 6. pp. 314-331. December 1974.

[2] D'Aquino, Stefano. *AD8029 Low Power Rail to Rail Operational Amplifier Design Review*. Unpublished. February 2003.

[3] Roberge, James K. *Operational Amplifiers: Theory and Practice.* Wiley, New York. October 1975.