PID Control of a Three Phase Photovoltaic Inverter Tied to a Grid Based on a 120-Degree Bus Clamp PWM

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Abstract: This paper presents a new operating type of a three phase photovoltaic PID current control system connected to the low voltage distribution grid. This operating type introduces a 120-degree bus clamp PWM control method (120° BC-PWM). A 120° BC-PWM is a special switching sequences technique employing bus clamp sequences that use only one phase under a PWM and PID control state every 60° while the other phases are being clamped. The BC-PWM method was used to generate six PWM signals to control a three phase inverter system every 60° with constant power input and a small dc link film capacitor. The main objective of this paper is to use new PWM techniques with a PID current control method to reduce the switching losses of three phase inverters. The losses were reduced to 1/3th for each transistor by reducing the time operation for each transistor. The simulation results of the BC-PWM method show an improvement in the performance of the three phase inverter system connected to the grid. Simulation setup of the system obtained is built by using a SiC MOSFET, 5 kVA, 400 V line-line and 25 kHz switching frequency. The PID control is not continuously active for each phase but is operational in 60° and saturated at 120° in a half period. Following a proper tuning of the windup, it recovers very easily.

Keywords: PID, three phase inverter, current control, 120-degree bus clamp, PWM, SIC MOSFET.

1. INTRODUCTION

Three phase inverters are the basic part of many applications in power electronic systems, including dc and ac transmission systems, dc energy storage, as well as three phase inverters for renewable energy applications connected to the low voltage grids. In general, three phase inverters are classified into two types based on the inverter operation control: (a) current source inverter (CSI) and (b) voltage source inverter (VSI) (Bozalakov et al., 2015; 2016; Moranchel et al., 2017).

The different pulse width modulation (PWM) programming methods depend on the carrier. PWM methods are a useful approach in most applications due to the characteristics of the output waveform (with low distortion of the injected currents) (Colak et al., 2016; Udakhe et al., 2016). There are two main techniques of PWM implementation: the digital technique and the cross intersection (natural sampling) technique. Controllers based on space vector modulation, first transform the three phases (abc) into two phases (dq). The natural sampling technique uses the natural reference frame and the carrier to generate the PWM signals and this technique is used in the inverter control proposed in this article. Typically, some headroom in voltage needs to be provided between the DC link and the peak value of the grid voltage. In this paper, it will be shown that voltage headroom is not needed if the DC link is modulated and the phase currents are directly modulated together with the input power which simplifies the control strategy because no transform to dq frame is required.

In general, the pursuit is to increase the efficiency of three phase inverters by reduced losses of components. The sum of switching losses and conduction losses are the total energy losses in semiconductor components (Aganah et al., 2015; Fujita, 2010). On one hand, the conduction losses depend on the manufacture properties of the transistors. On the other hand, switch losses occur during ON/OFF transistor operation (Mnati et al., 2016; Van Den Bossche et al., 2014; Yao et al., 2015). Three different strategies may reduce the switching losses. The first strategy is to reduce the transistor current or the voltage across the transistor (collector-emitter) is close to zero during ON/OFF processes (soft switching). In the second strategy, different types of modulation may result in lower switching edges by lowering the effective switching frequency to reduce losses. The third strategy is reducing losses by using DC link bus clamp techniques. The aim of this article is to design and simulate a new PID controller technique with the features of a reduced switching loss and increased efficiency. The 120° BC-PWM control method has been designed as a three phase inverter connected to the low voltage grid under PID current control. Every 60°, only one of the three phase legs operate under PID current control regulation with switching pulse width modulation and the other two legs (phases) are completely ON or OFF. Simulation setup of the system is built by using a SiC MOSFET (CMF10120D) transistor, 5 kVA,400 VLL and 25 kHz as a switching frequency.

The rest of the paper is organised as follows: Section 2 presents the proposed system block diagram configuration technique of a 120º BC-PWM; Section 3 presents the control method; the simulation results of the above method are presented and discussed in Section 4; and finally, Section 5 presents conclusions.

2. 120º BC-PWM BLOCK DIAGRAM

Fig.1 shows the block diagram of the three phase photovoltaic inverter used in this research. The AC terminal of the inverter is connected directly to the grid (400V line-to-line and 50Hz) through a three phase L-Filter. The photovoltaic is connected to a DC-DC converter which is connected to the DC terminals on the inverter. The DC link capacitor is consisted of a small value film capacitor. The properties of the inverter are listed in Table 1. The phase lock loop (PLL block) in is used to generate the three reference currents for the system control.

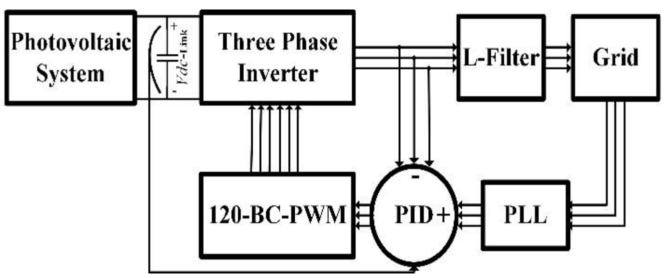


Fig.1. Block diagram of a three phase photovoltaic system.

Table 1. System parameter

Parameter	Value
Grid Voltage	400V(L-L)
Grid Frequency	50Hz
Filter Inductor	2.5mH
Switching Frequency	25kHz
Film Capacitor	8 µF

For the PWM of the three phase inverter, a new PID current control method is used to generate the six PWM signals for the three phase inverter in this work. This method is called a 120-degree bus clamp PWM control method (120° BC-PWM). The 120° BC-PWM method clamps for 120º ON or OFF duration every half cycle of each grid phase voltage. Fig. 2 depicts the switching states of the three phase inverter presented in Fig 5. Fig. 2 also depicts the intervals where the transistors are ON and OFF as well as the PWM interval. Furthermore, the control signals for all transistors are shown in Fig. 2 a) to c).

The voltage across the DC link film capacitor (V_{dc}) for the 120° BC-PWM method shown in Fig. 3a depends on the three phase grid voltage waveforms in that are depicted in Fig. 3b. The waveform of the voltage across the DC link capacitor V_{dc} in Fig. 3a has the same waveform as a three phase bridge rectifiier and the frequency is six times that of the fundamental frequency in Fig. 3b. Equation 1 presents the minimum and maximum voltage across the DC link capacitor, and the calculation depends on the grid line-to-line voltage.

$$V_{dc}(max.) = \sqrt[2]{2}V_{LL}$$
$$V_{dc}(min.) = \sqrt[2]{\frac{3}{2}}V_{LL} \tag{1}$$

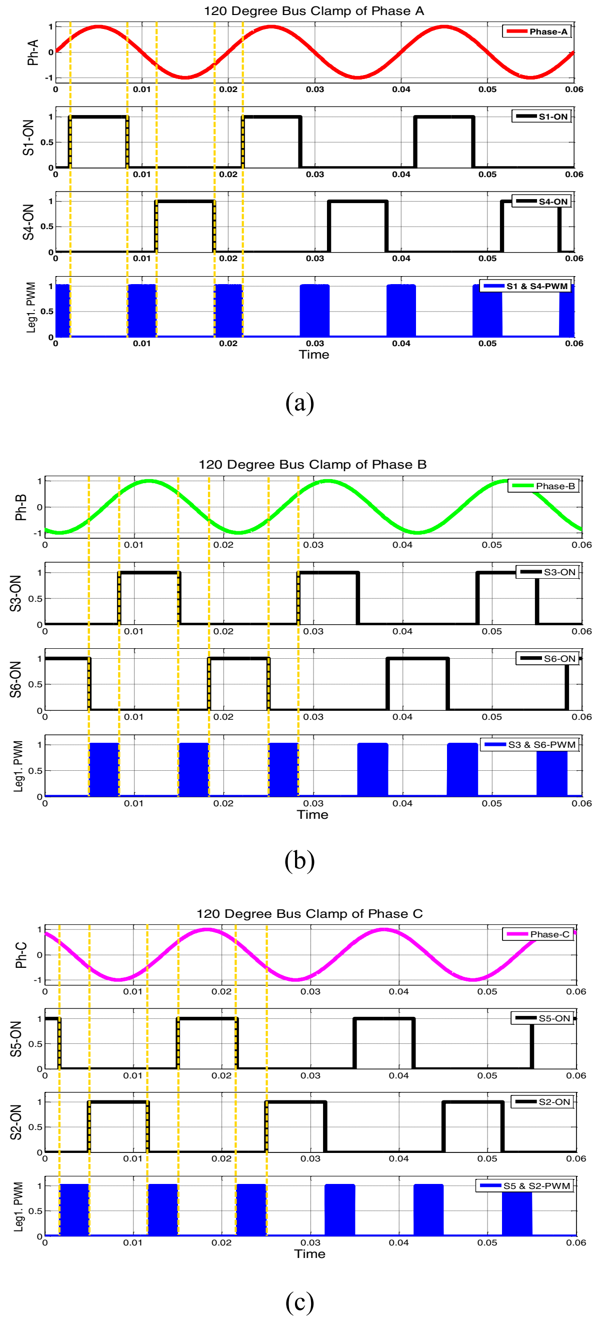
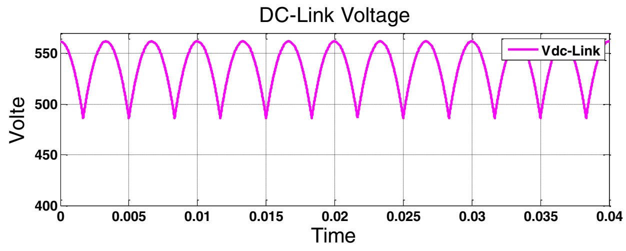


Fig. 2. BC-PWM with PID current control waveforms: (a) phase A; (b) phase B; (c) phase C.

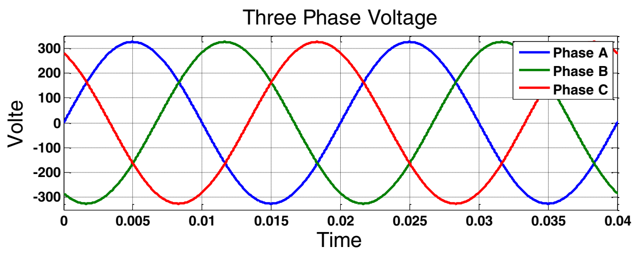
3. PID AND BUS CLAMP PWM CONTROL METHOD

In Fig. 4, a basic PID bus clamp current control theory was developed and implemented in the current source inverter.

In this theory, three independent current controllers are used – one for each phase inverter. All three output currents of the inverter are individually detected and compared with the corresponding phase current references. The reference currents are generated by using the PLL signals and scaled according to the available power from the renewable source as shown in Fig. 4 a). The resulting errors are directly used for the PID current control to generate the PWM signals for SiC MOSFET through 120º BC-PWM theory.



(a)



(b)

Fig. 3. DC-Link voltage: (a) dc link voltage V_{dc}; (b) three phase grid voltage.

The three phase PID current source inverter depicted in Fig. 1 and Fig. 4 is controlled by a six-inverter configuration and six switches. The six inverter states can be transformed into six corresponding bus clamp PWMs. In each state, only one leg is under PWM and PID current control states and the others are in ON or OFF states. The relationship between the switching states and the 120º bus clamp PWM control method is given in Table 2 and Fig.5. Fig. 5 presents the first state of the 120º BC-PWM.

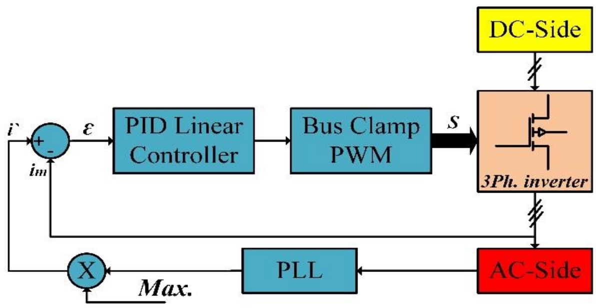
According to Fig. 5 and Table 2, every 60º, only one phase is under PID current control and can calculate the duty ratio (D_{xx}) and phase current. Fig. 5 and equations 2 and 3 are an example of how to calculate (D_{a1}), i_{b1} and i_{c1} for phase A depending on the grid voltage: ($V_{PhB} \geq V_{PhA} \geq V_{PhC}$) and ($0 \geq \theta \geq \pi/6$ & $11\pi/6 \geq \theta \geq 2\pi$. Fig. 5 shows the leg A under PWM and the lower transistor of phase B. The upper of phase C is ON and the upper transistor of phase B and lower of phase C is OFF. Equations 2 and 3 can be repeated with the same sequence of every 60º to calculate the (D_{a1}, D_{b1}, D_{b2}, D_{c1} *and* D_{c2}) and (i_a, i_b and i_c). The 120º bus clamp ON/OFF is in the centre of the half cycle. The PWM for each phase is 120º divided into two 60º, which is 30º around the zero crossing point for each phase.

$$D_{a1} = \frac{V_a - V_b}{V_{dc}} = \frac{V_a - V_b}{V_c - V_b} \tag{2}$$

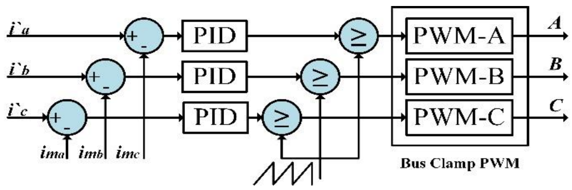
$$i_{b1} = i_{inv} + D_{a1} i_{a1}$$
$$i_{c1} = i_{inv} + (1 - D_{a1}) i_{a1} \tag{3}$$

4. SIMULATION RESULT OF BC-PWM

For the PID current control in Fig. 1 and Fig. 5, the system was designed according to MATLAB PID parameters K_P=3.5, K_I=3.5 and K_D=0, so that the simulation results can be divided into two types of signals (input and output side signals).

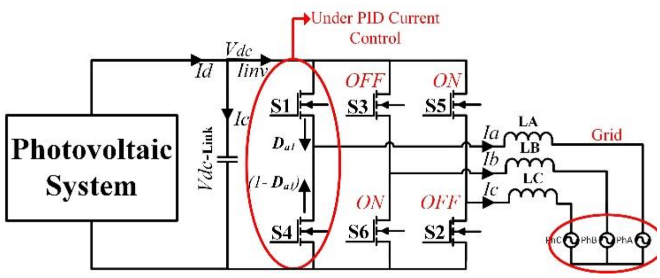


(a)



(b)

Fig. 4. Basic PID bus clamp current control theory: (a) Full control system; (b) PID and BC-PWM system.



(a)

Fig. 5. Configuration of 120º BC-PWM under PID current control method.

4.1 Input simulation results (DC link side)

The simulation results of the DC link side waveforms of the 120º BC-PWM and PID current control method are divided into inverter switched signals (S1 to S6), inverter current, supply current, DC link capacitor current, and voltage across the film capacitor, as shown in Fig. 6 and Fig. 7. Fig. 6 shows the simulation result of the generated six PWM signals for a three phase 120º BC-PWM and PID current control method under a steady state condition. The PWM for each phase is 60º around the zero-crossing point (30º before and 30º after zero-crossing) for each phase and the legs work as complementary PWM for upper and lower transistors.

4.2 Output simulation results (AC link side)

All the simulation results of the AC side signals under 120º BC-PWM and PID current control method are presented in Fig. 8. The simulation results of the AC side are divided into three phase output currents, as shown in Fig. 8(a). The three phase voltages at the point of common coupling are shown in Fig. 8(b) and phase A line to neutral of the inverter is shown in Fig. 8(c). The acceptable compensation waveforms between the measuring current and reference current are presented in Fig. 9 and it can be seen that both the reference and measured currents match very well. Hence, the steady-state error will be very small.

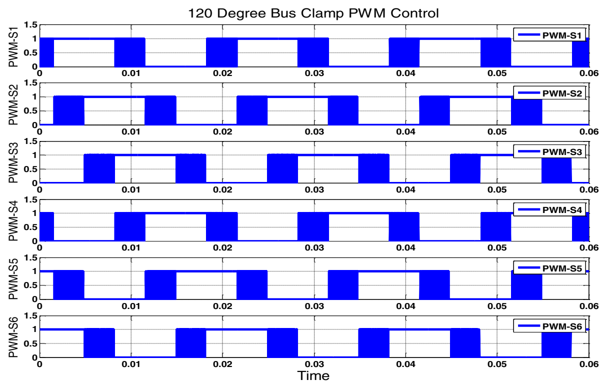
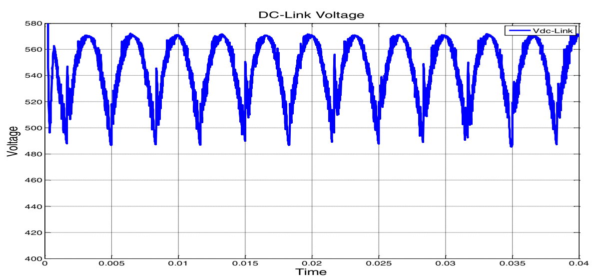
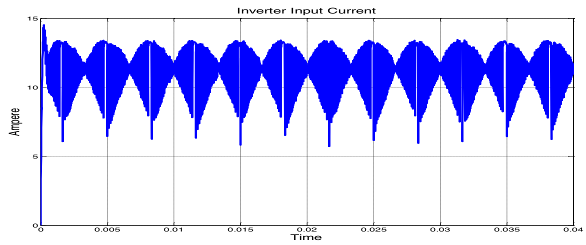


Fig. 6. Six PWM under BC-PWM and PID current control.



(a)



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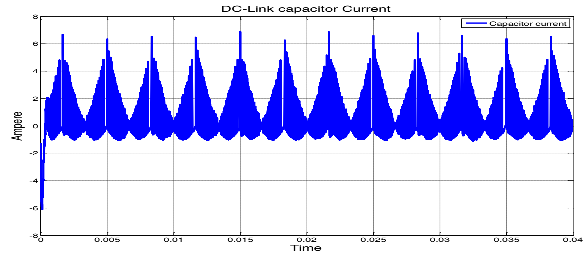

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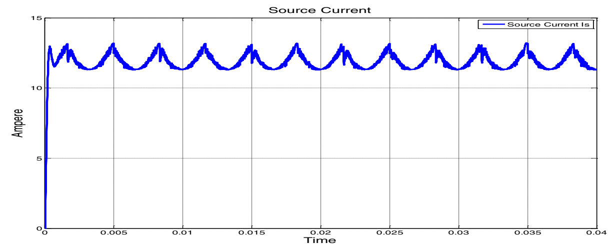
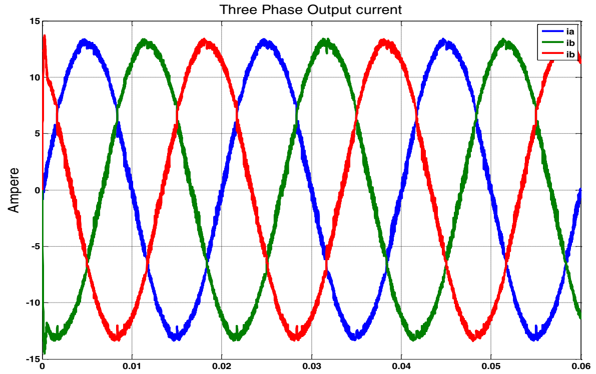


(d)

Fig. 7. Input side simulation result: (a) dc-link voltage (V_{dc}); (b) input current of the inverter (I_{inv}); (c) capacitor current (I_C); and (d) supply input current (I_d).

Table 2. 120º bus clamp switching states

One Cycle 2π	**Leg A S1 and S4**	**Leg B S3 and S6**	**Leg C S5 and S2**
$0 \geq \theta \geq \pi/6$ $11\pi/6 \geq \theta \geq \pi$	PWM	OFF – ON	ON - OFF
$\pi/6 \geq \theta \geq \pi/2$	ON - OFF	OFF – ON	PWM
$\pi/2 \geq \theta \geq \pi/6$	ON - OFF	PWM	OFF – ON
$5\pi/6 \geq \theta \geq 7\pi/6$	PWM	ON - OFF	OFF – ON
$7\pi/6 \geq \theta \geq 3\pi/2$	OFF – ON	ON - OFF	PWM
$3\pi/2 \geq \theta \geq 11\pi/6$	OFF – ON	PWM	ON - OFF



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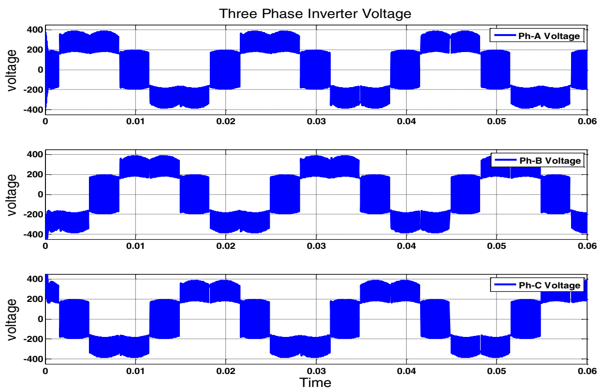

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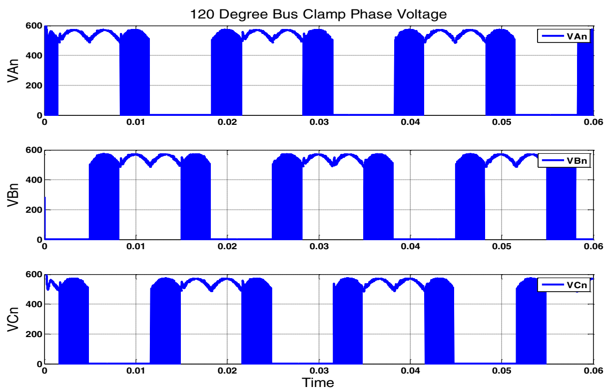


(c)

Fig. 8. The simulation output waveform (AC side): (a) three phase lines current; (b) three phase voltage; and (c) three phase voltage to negative DC link of the inverter.

The simulation results of total harmonic distortions are depicted in Fig. 10. As can be seen, when the 120° BC-PWM is used, the THD level is acceptable and is below 2.333% on average for the three phase system.

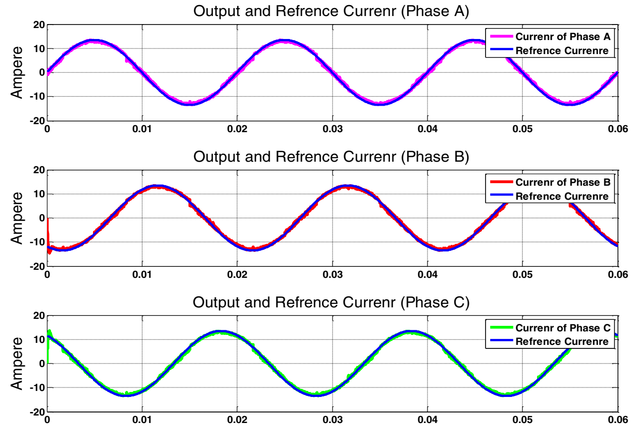
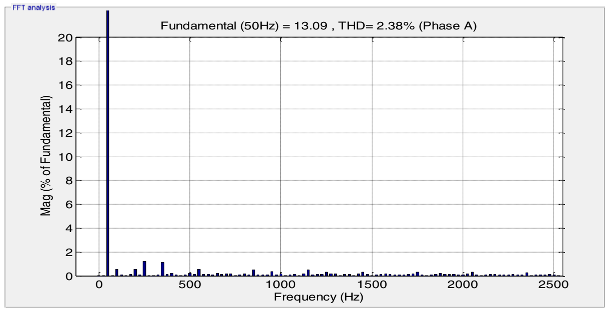
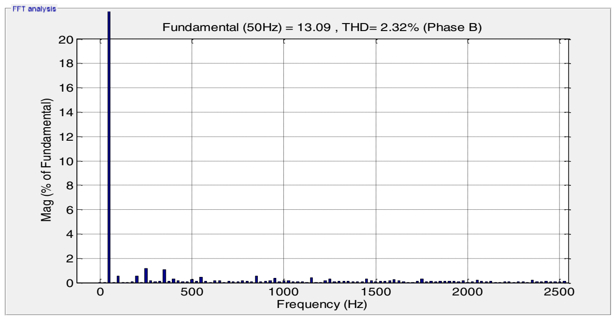


Fig. 9. Three phase measuring current and reference current



(a)



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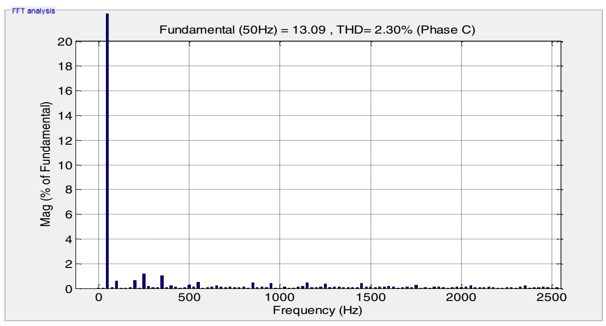

(c)

Fig. 10. Three phase THD: (a) phase A; (b) phase B; and (c) phase C.

5. CONCLUSIONS

This paper has successfully illustrated a new technique called 120° bus clamp PWM control method using PID current control (120° BC-PWM). The 120° BC-PWM method is developed by an independent PID current controller on the three phase photovoltaic inverter connected to the grid. In this PID current control, every 60°, only one of the three phase legs operate under current control regulation with PWM and the other two legs (phases).

From the above MATLAB simulation results, it is clear that the current controller is performing well and is able to track the reference currents with very small steady-state error. Also, an acceptable THD level for the three phase line currents is obtained (2.33%) and the switching losses were reduced by a factor of 1/3 for each transistor under the 120° bus clamp PWM control method.

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Alex Van den Bossche. received his M.Sc. and Ph.D. degrees in electromechanical engineering from Ghent University Belgium, in 1980 and 1990, respectively. He has worked at the university’s Electrical Energy Laboratory. Since 1993, Dr. Bossche is a professor at the same university in the same field. His research is in the field of electrical drives, power electronics on various inverter types and passive components, and magnetic materials. He is also interested in renewable energy conversion. He is an author of the book entitled “Inductors and Transformers for Power Electronics”. He was a starter of the spin-off companies Inverto n.v. (1990) and recently Alenco n.v. (2009). He is an IEEE member since 2000 and a senior member of IEEE since 2003.